TIGP lecture, NTU 070501

Advanced Device Fabrication Techniques

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Outline:

1 State-of-the-art device fabrication techniques

  Future light sources: EUV and e-beam

2 e-beam lithography

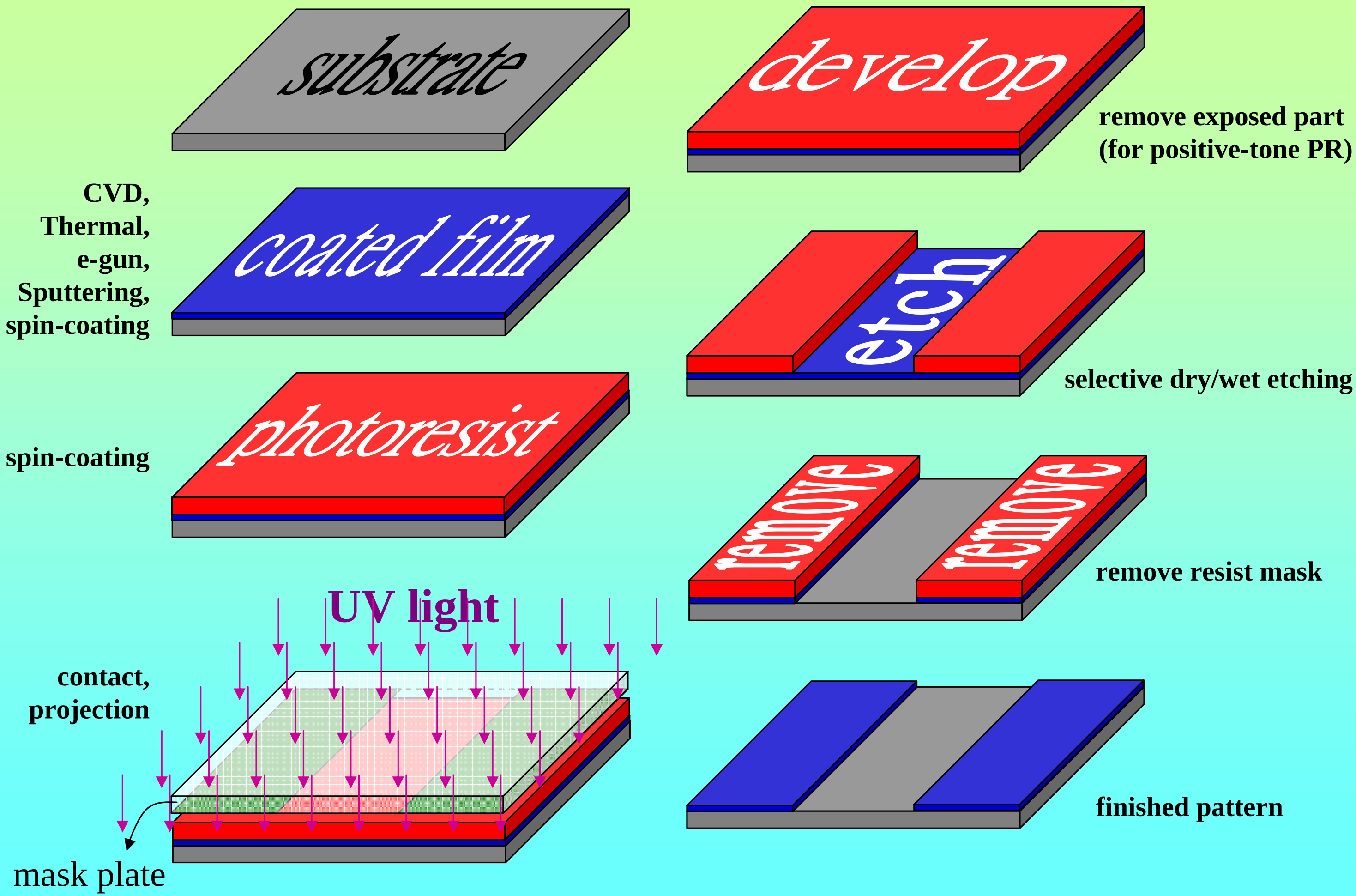
3 Examples:

  nano-pore based point contact devices

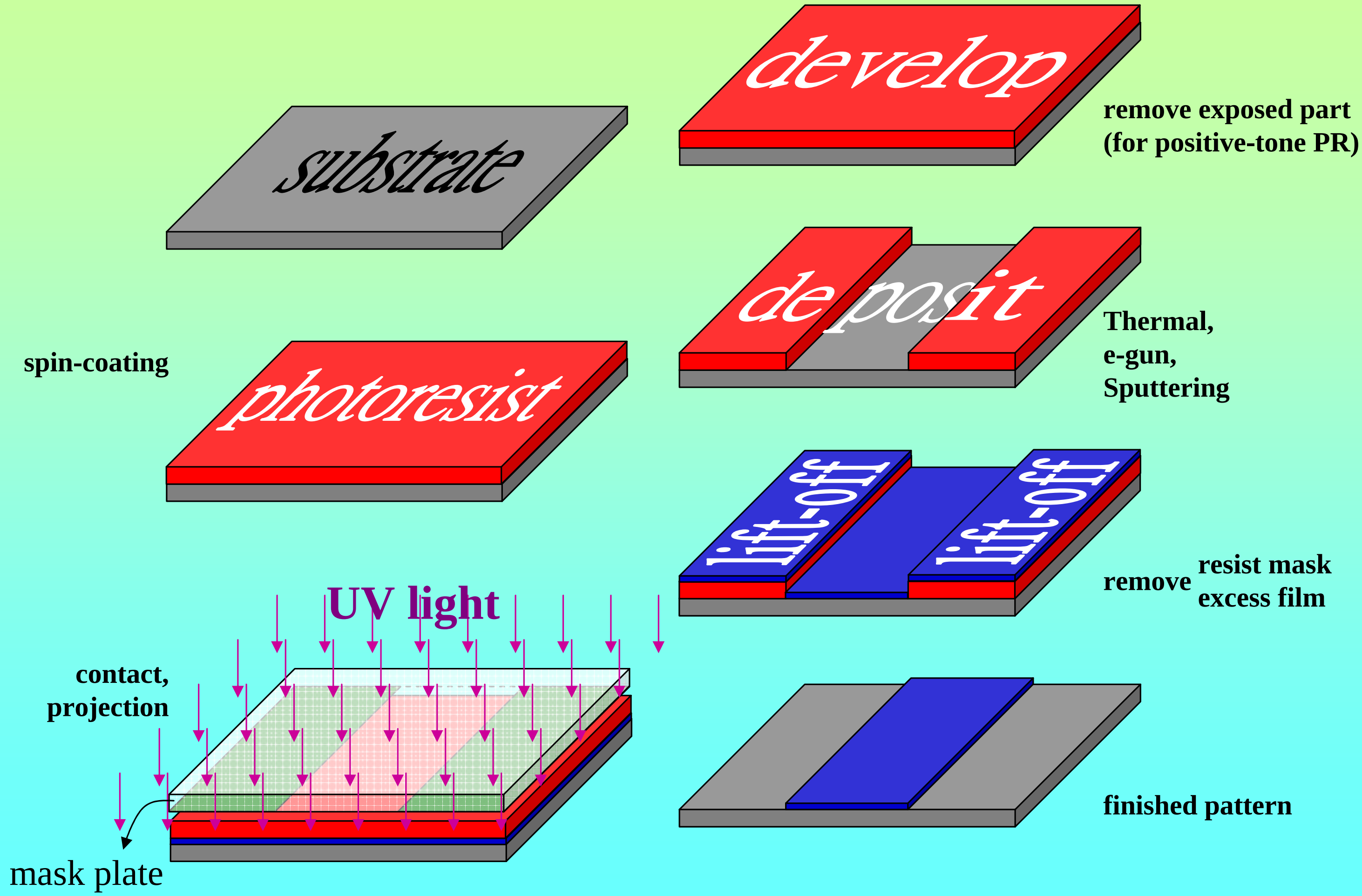
  nano electronic devices

Lithography = Pattern transferring

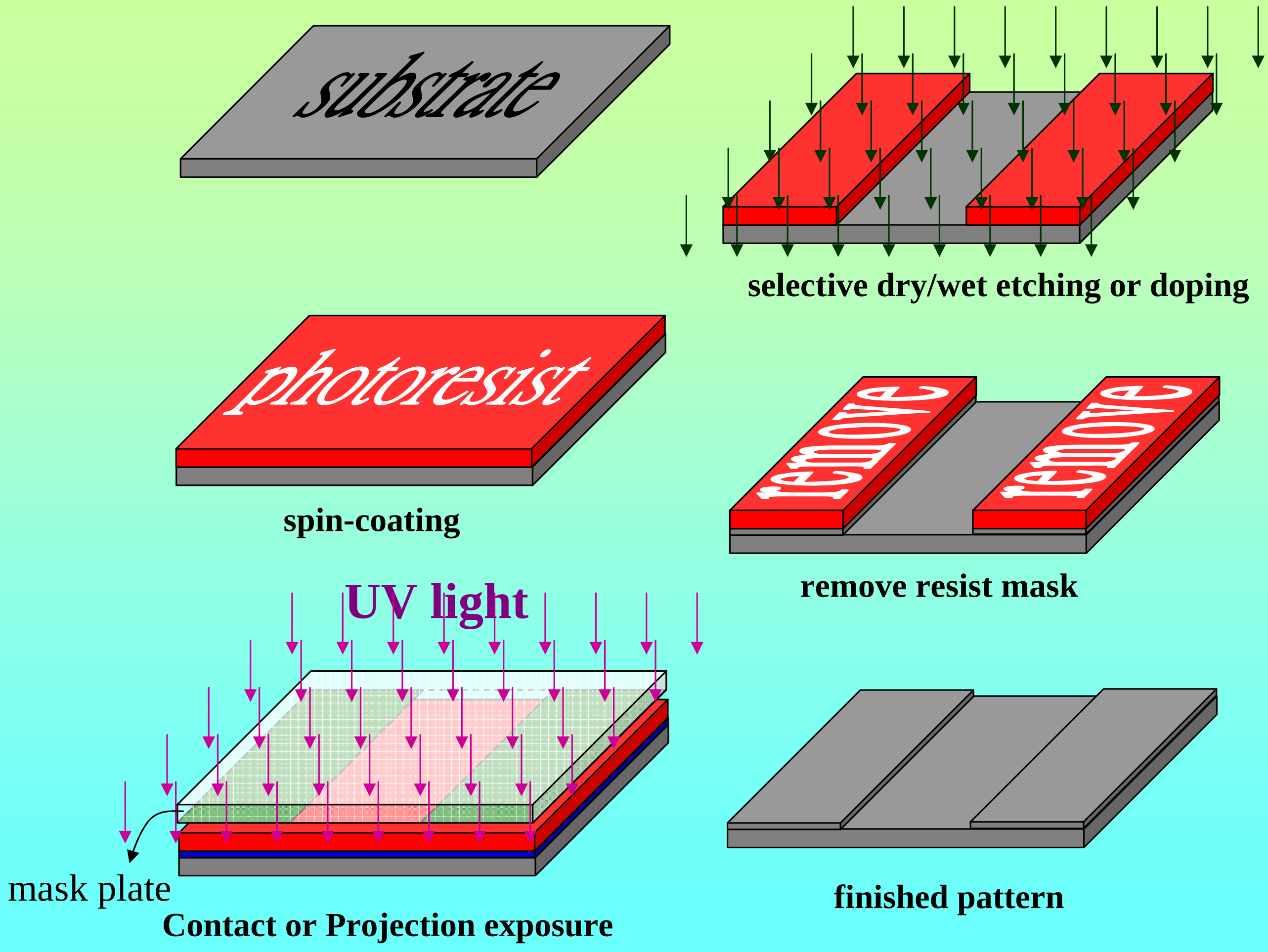
Standard etching process



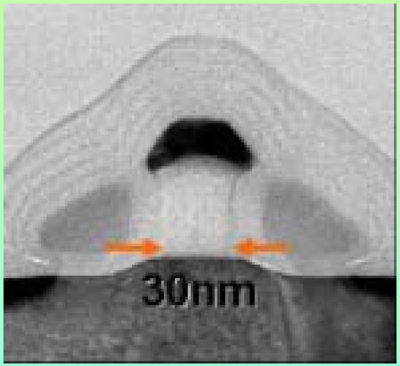
Complementary process: lift-off



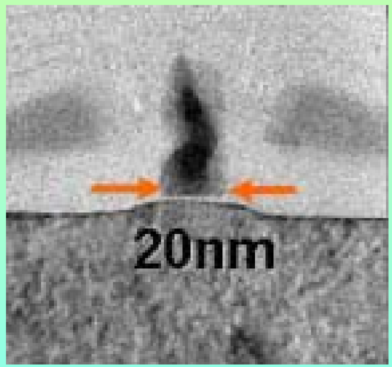
Substrate treatment process



Experimental transistors for future process generations

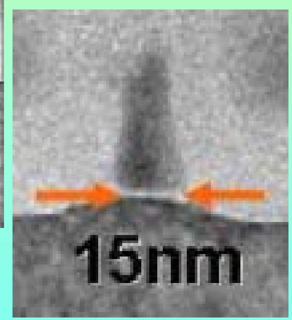


65nm process
2005 production

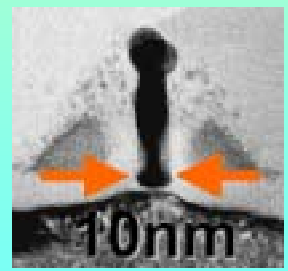


45nm process
2007 production

CMOS
0.8 nm conventional gate oxide



32nm process
2009 production

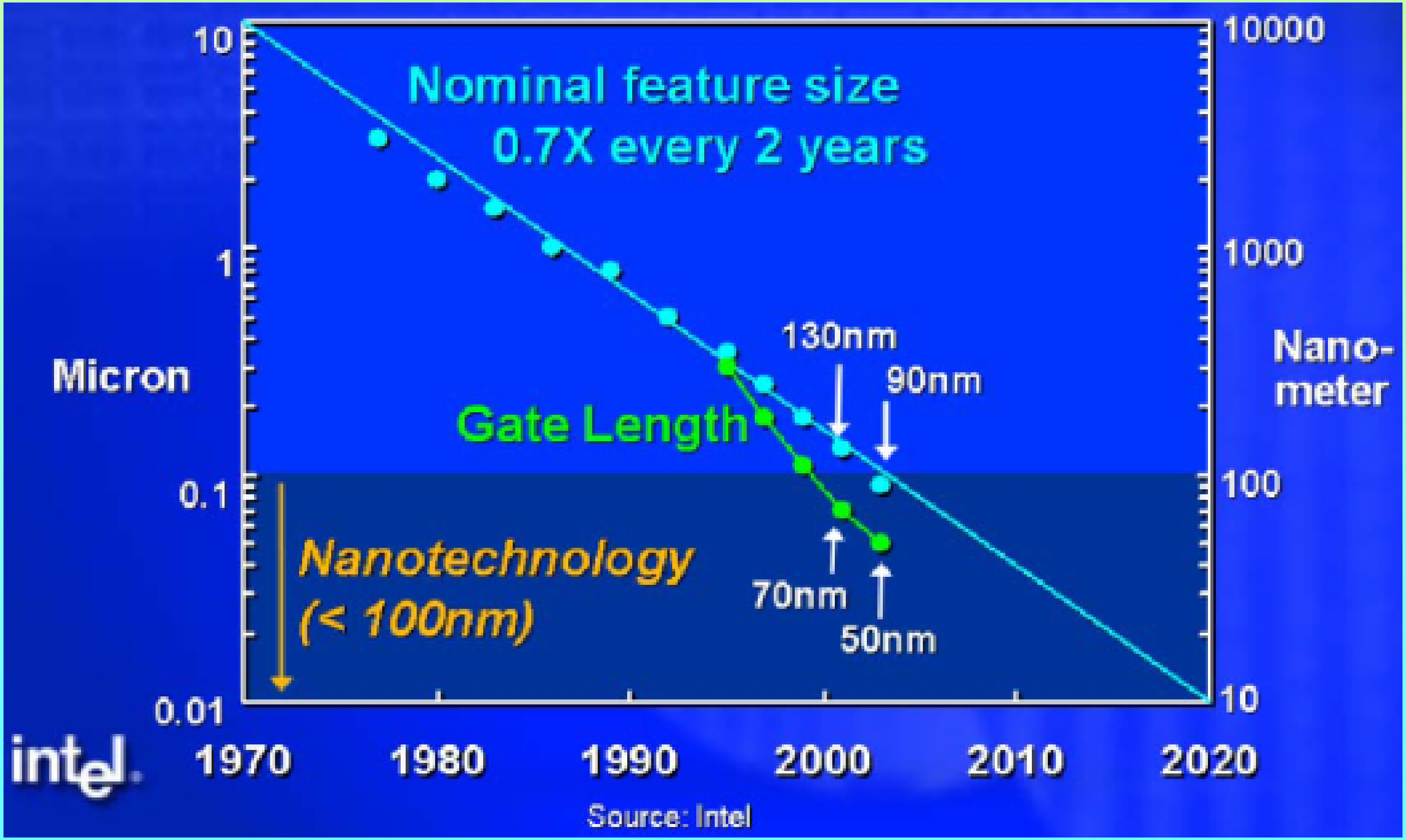


22nm process
2011 production

Intel C. Michael Garner

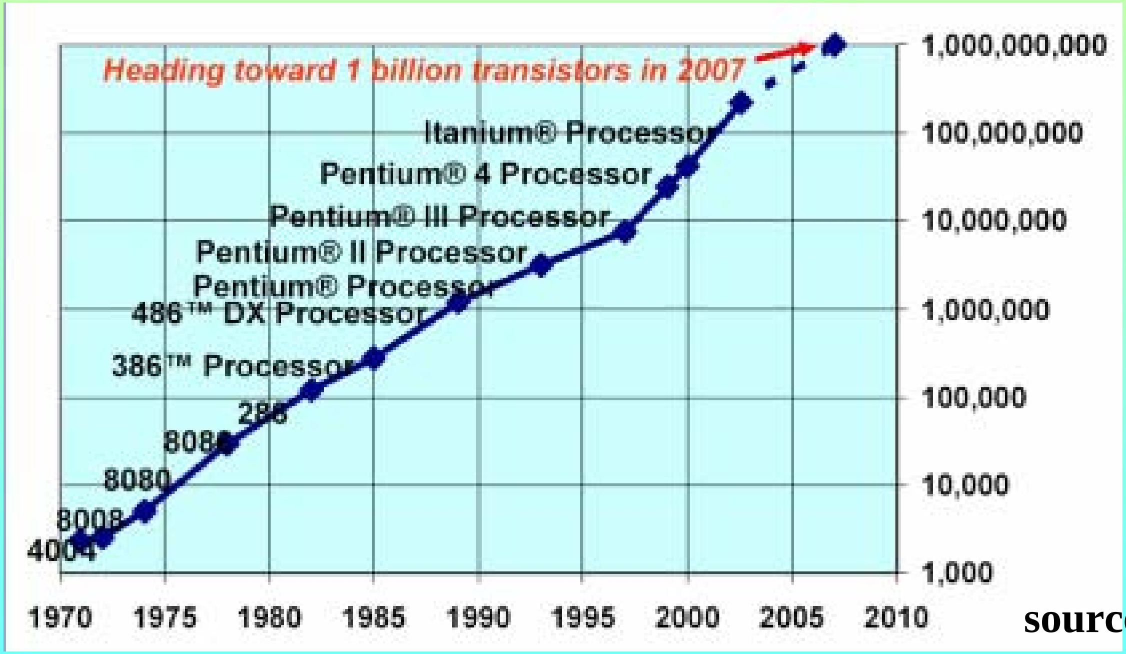
Moore's Law:

a 30% decrease in the size of printed dimensions every two years



Large circuit functions on a single semiconductor substrate =

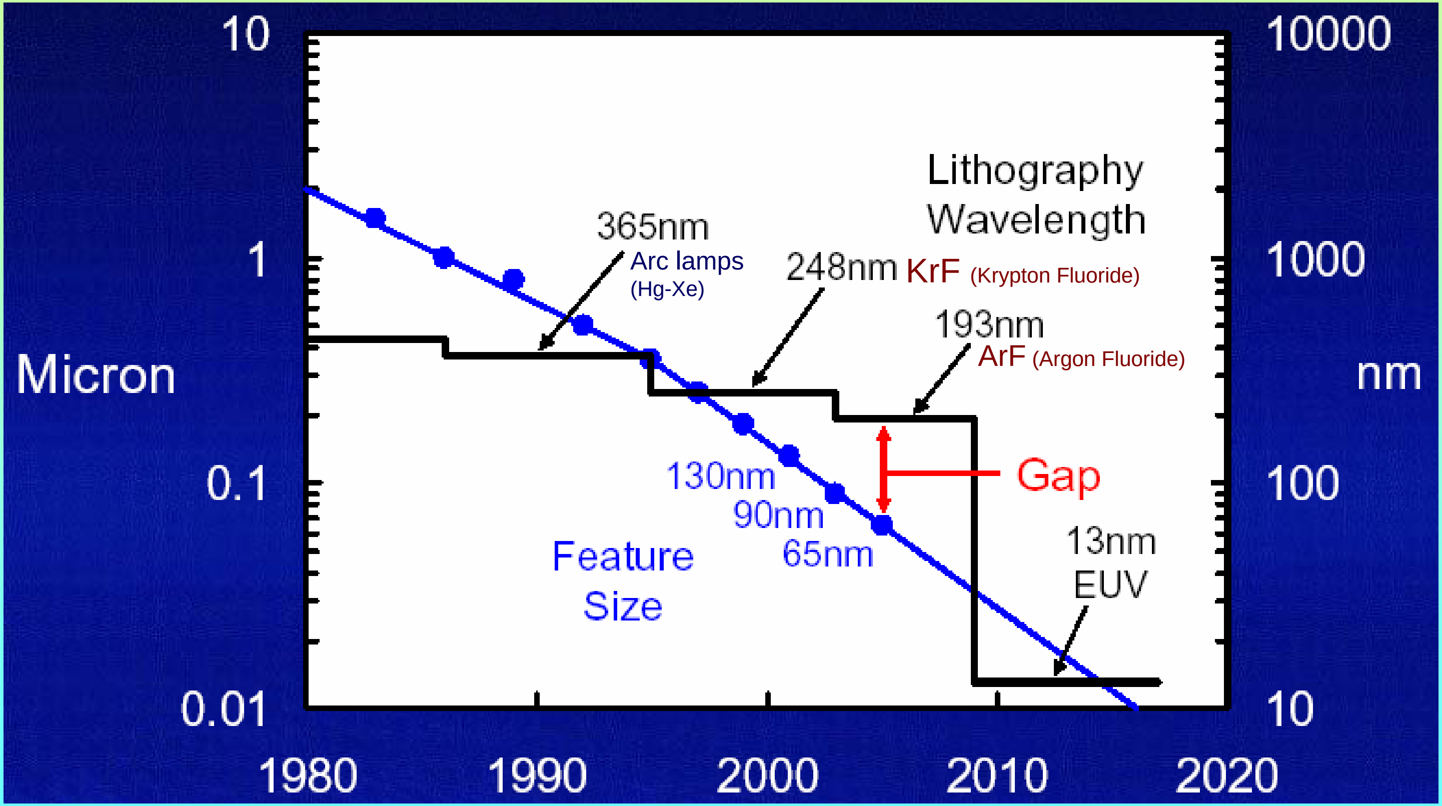
Reduced cost !



source: Intel

>220M Transistors Integrated into Devices Produced Today

SOURCES OF RADIATION
FOR MICROLITHOGRAPHY



Minimum feature size is scaling faster than lithography wavelength
Advanced photo mask techniques help to bridge the gap

Mark Bohr, Intel

The Ultimates of Optical Lithography

Resolution: $R = k_1 (\lambda/NA)$

$NA = \sin\theta$ = numerical aperture

K_1 = a constant for a specific lithography process

smaller K1 can be achieved by improving the process or resist contrast

Depth of Focus $DoF = k_2 (\lambda/NA^2)$

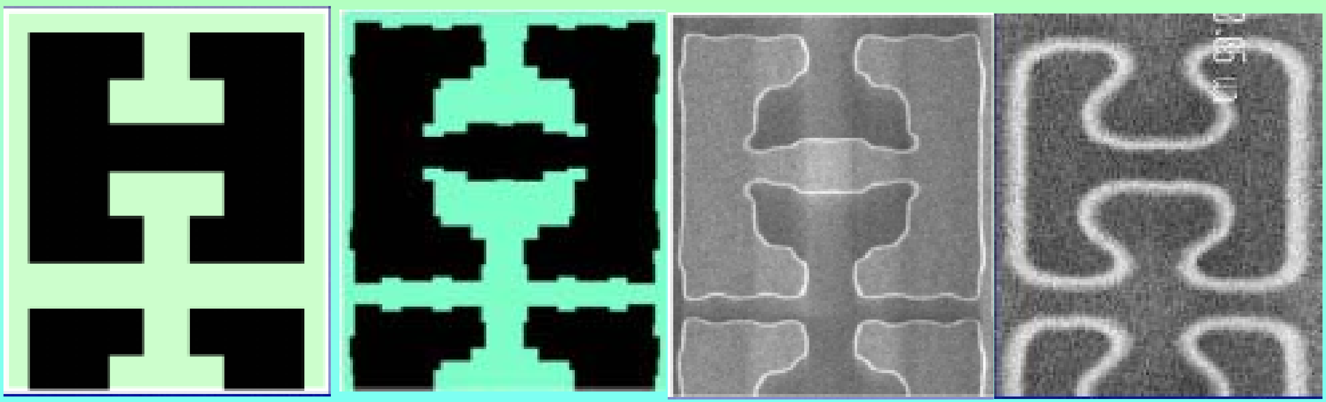
Calculated R and DoF values

UV wavelength	248 nm	193 nm	157 nm	13.4 nm
Typical NA	0.75	0.75	~~0.75~~	0.25
Production value of k_1	0.5	0.5	~~0.5~~	0.5
Resolution	0.17 µm	0.13 µm	~~0.11 µm~~	0.027 µm
DoF (assuming k_2 = 1)	0.44 µm	0.34 µm	~~0.28 µm~~	0.21 µm

P.F. Carcia et al. DuPoint Photomasks, Vacuum and Thin Film (1999)

Optical Proximity Correction

used in 90 nm (193nm) production line

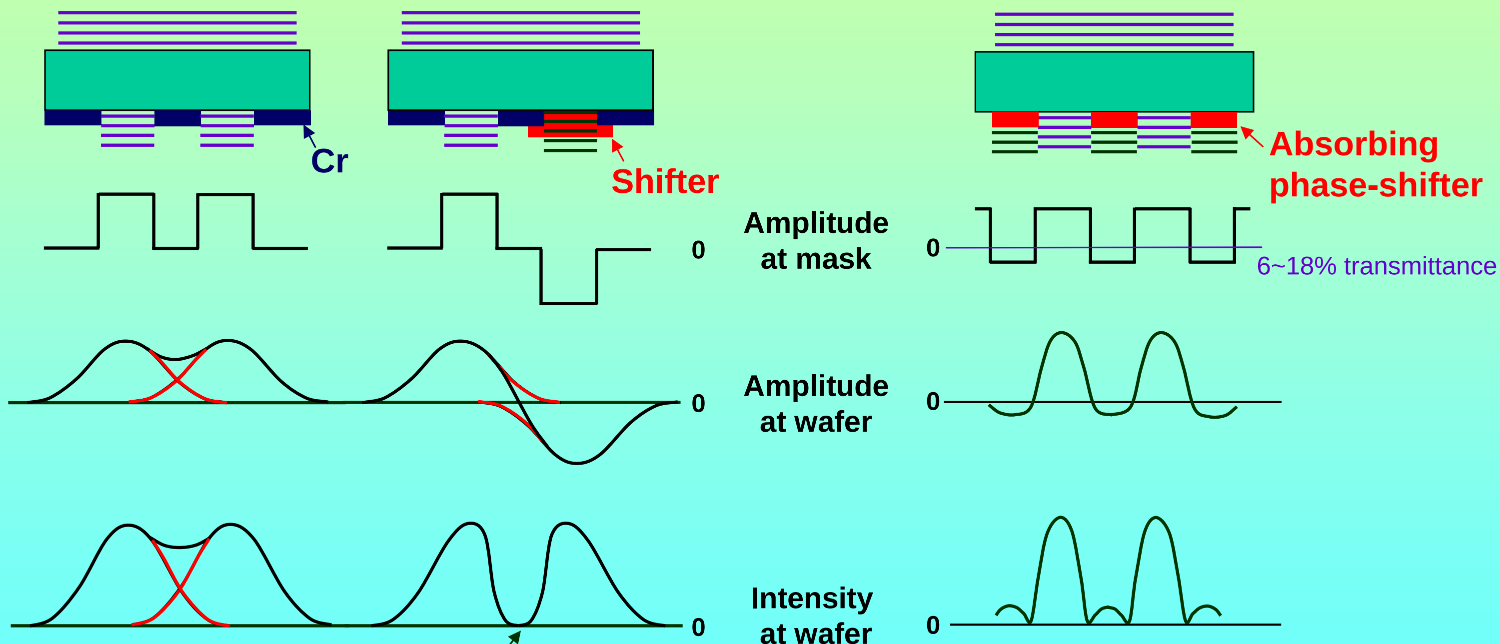


Drawn structure **Add OPC features** **Mask structure** **Printed on wafer**

Mark Bohr, Intel

Two types of phase shift mask

Alternating aperture phase shift mask | **Embedded attenuating phase shift mask**



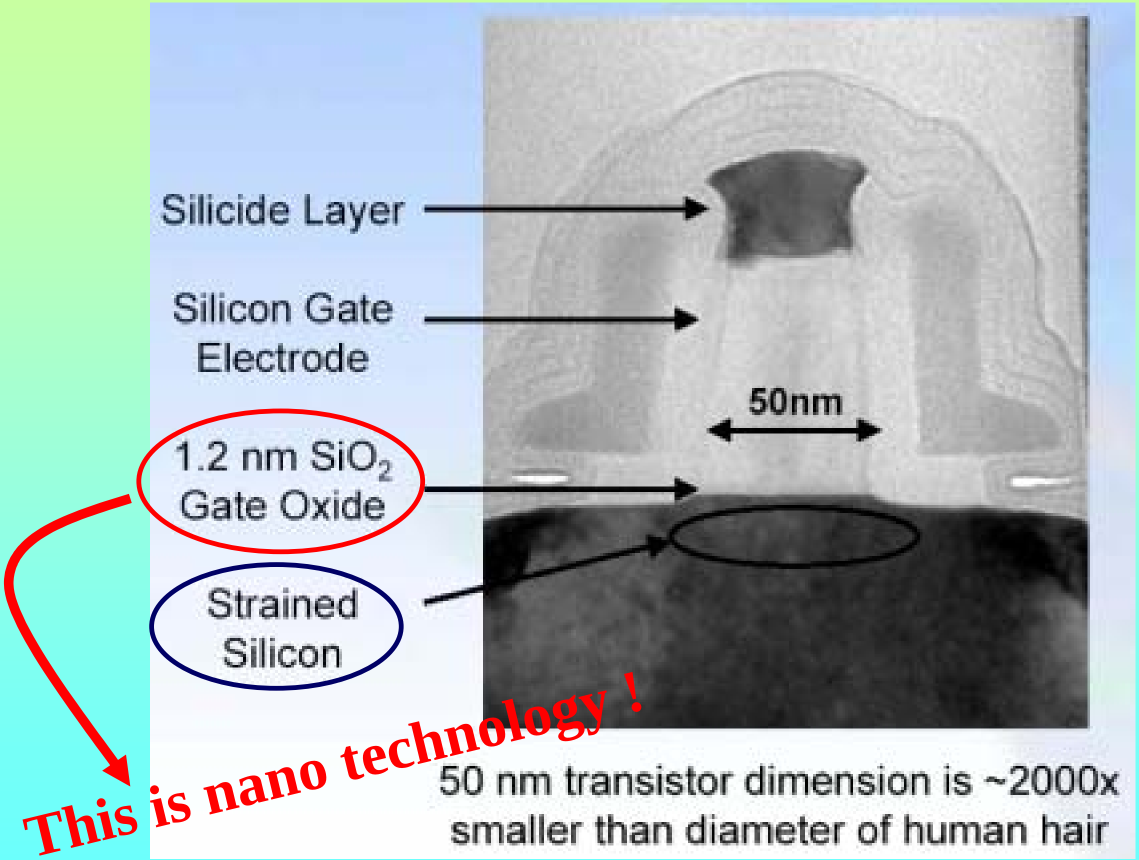
1. dark line appears at the center
2. Applicable only in limited structures

1. Can even improve DoF
2. Use $MoSi_xO_yN_z$, SiN_x or CrO_xF_y instead of Cr

Ref: P.F. Carcia et al. DuPoint Photomasks, Vacuum and Thin Film

Material Engineering
gains
importance !

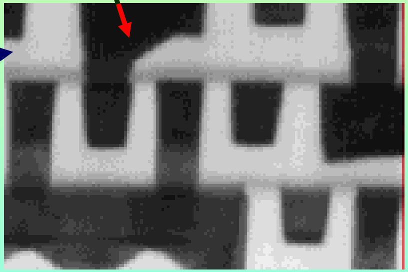
90 nm Generation Transistor



source: Intel develop forum
Spring, 2003

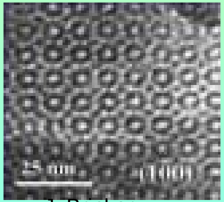
Nano materials will play an important role
in the silicon nanotechnology platform

Interconnectors with high electrical conductivity



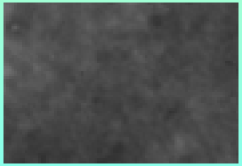
Low K interlevel Dielectric

High K gate oxide

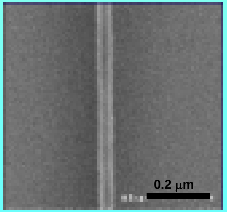


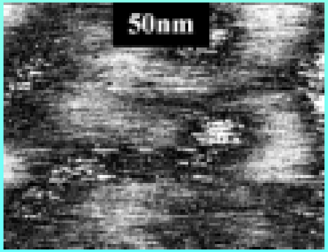
J. Brinker,
UNM/Sandia National Labs

Strained Si



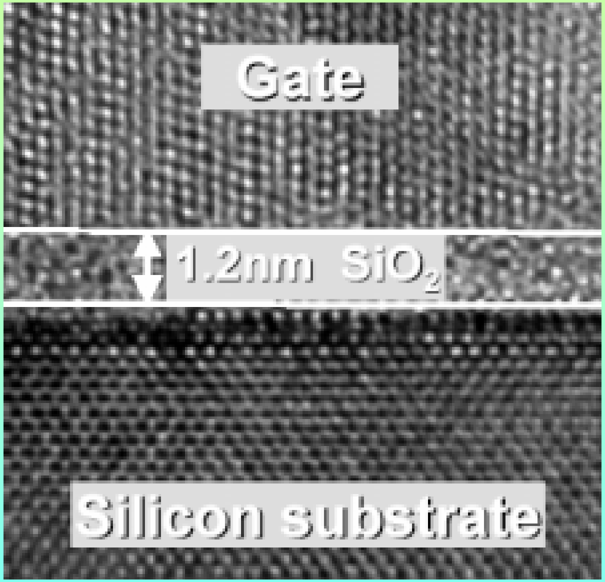
Photoresist

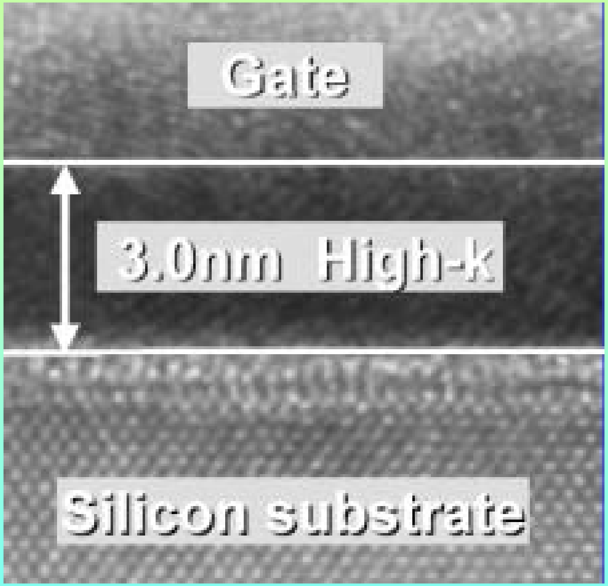




C. Michael Garner, Intel, Sept.16, 2003

Introduction of high-K gate dielectric





	90 nm process	**Experimental high-K**
Capacitance	1X	1.6X
Leakage	1X	<0.01X

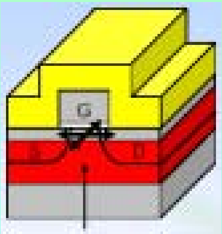
Carolyn Block, Intel

A message from Intel

Compress P-doped regions
by filling SiGe into carved trenches,
hole conduction increased by 25%

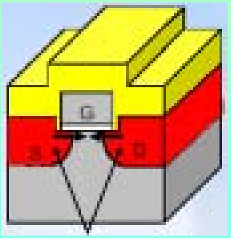
Stretch N-doped regions
by annealing SixNy cover layer,
electron conduction increased by10%

Traditional MOS



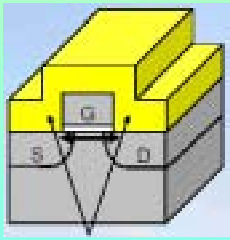
Graded SiGe layer

new PMOS



Selective SiGe S-D

new NMOS

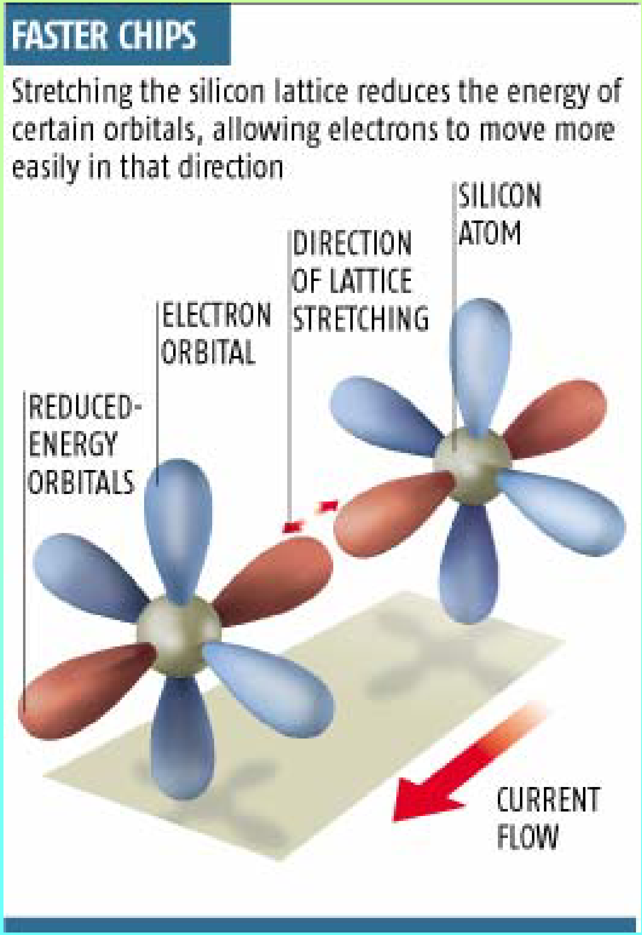


Tensile Si_3N_4 Cap

Strained silicon benefits

- **Strained silicon lattice increases electron and hole mobility**
- **Greater mobility results in 10-20% increase in transistor drive current (higher performance)**
- **Both NMOS and PMOS transistors improved**

Intel develop forum



http://www.newscientist.com/news/news.jsp?id=ns99994493

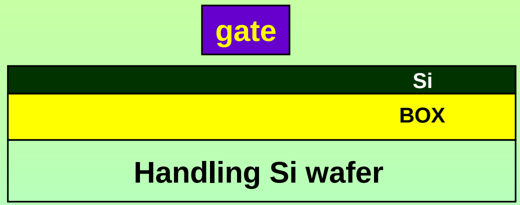
Introduction of new materials

1st Production	1997	1999	2001	2003	2005	2007	2009	2011
Process Generation	0.25 μm	0.18 μm	0.13 μm	90 nm	65 nm	45 nm	32 nm	22 nm
Wafer Size (mm)	200	200	200/ 300	300	300	300	300	300
Inter-connect	Al	Al	Al	Cu	Cu	Cu	Cu	?
Channel	Si	Si	Si	Strained Si	Strained Si	Strained Si	Strained Si	Strained Si
Gate dielectric	SiO_2	SiO_2	SiO_2	SiO_2	SiO_2	High-k	High-k	High-k
Gate electrode	PolySi	PolySi	PolySi	PolySi	PolySi	Metal	Metal	Metal

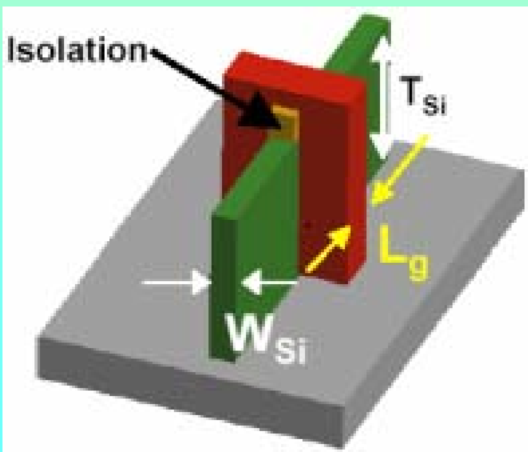
source: Intel develop forum

Three types of new Fully Depleted Transistors

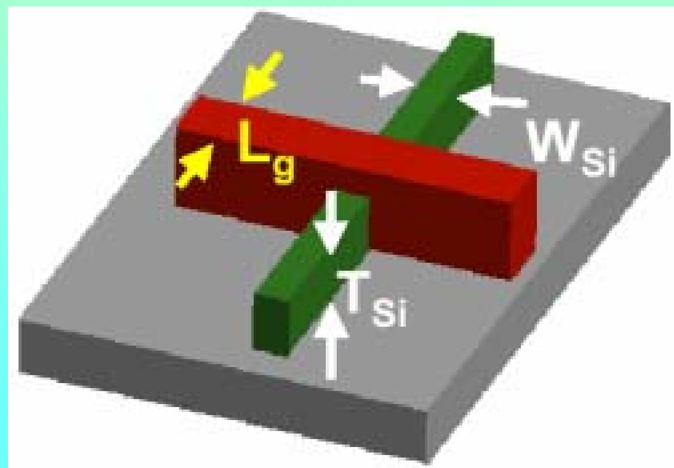
SOI wafer



Planar fully depleted SOI

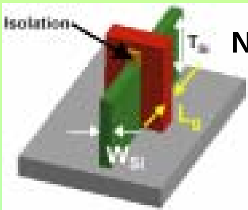


Non-planar Double-gate (FinFET)

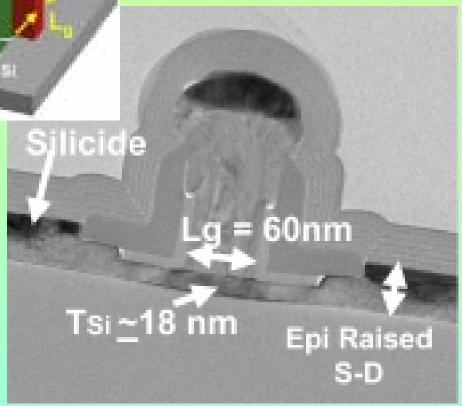


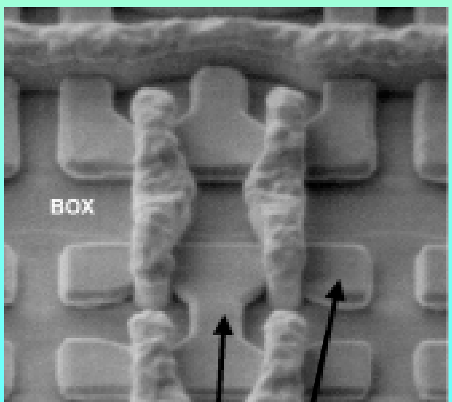
Non-planar Tri-gate

Fully Depleted Transistors made on SOI wafers



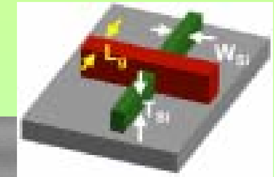
Non-planar Double-gate (FinFET)

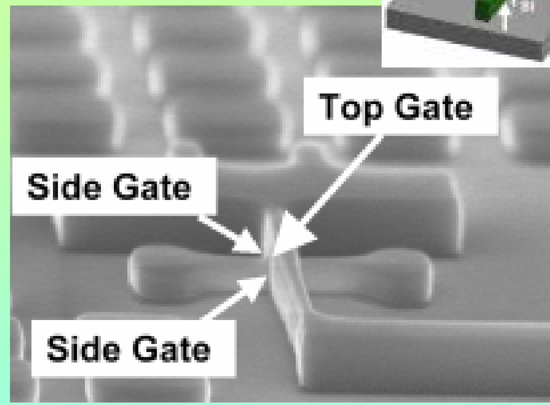


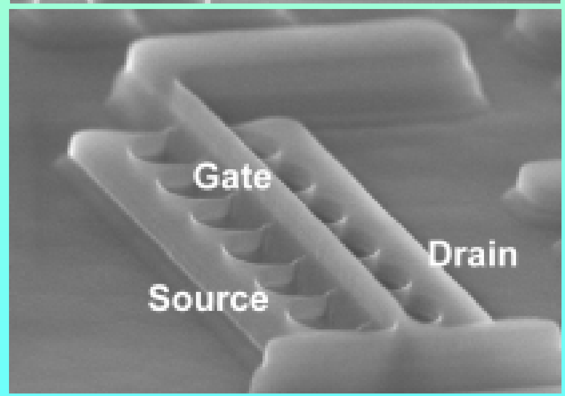


Raised S-D using Selective Epi-Si Deposition

Non-planar Tri-gate



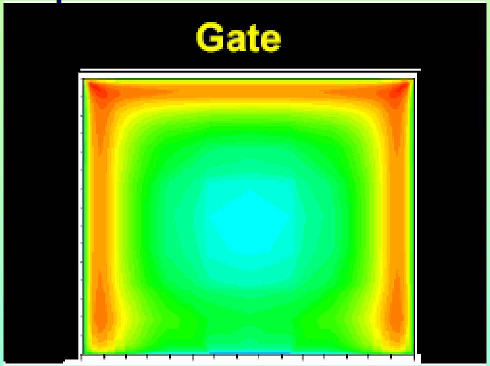


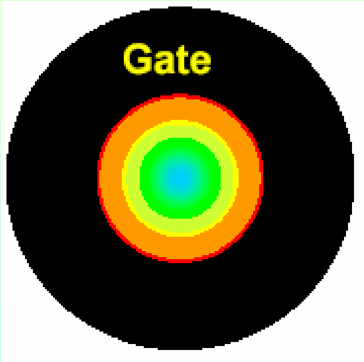


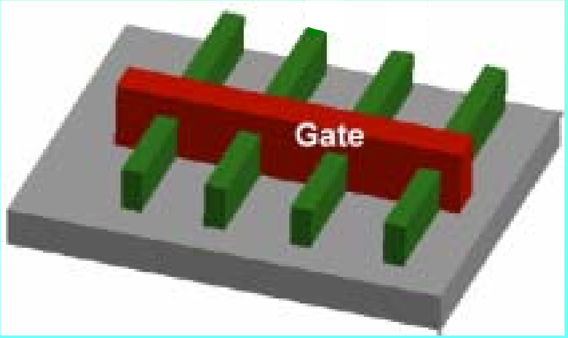
Robert Chau, Intel

From Tri-gate transistors to Nano-wire transistors

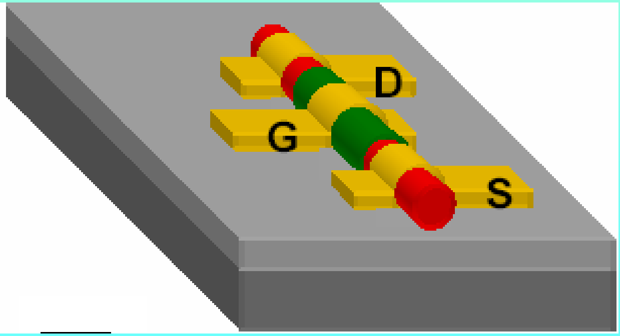
depletion electric field







Tri-gate transistor



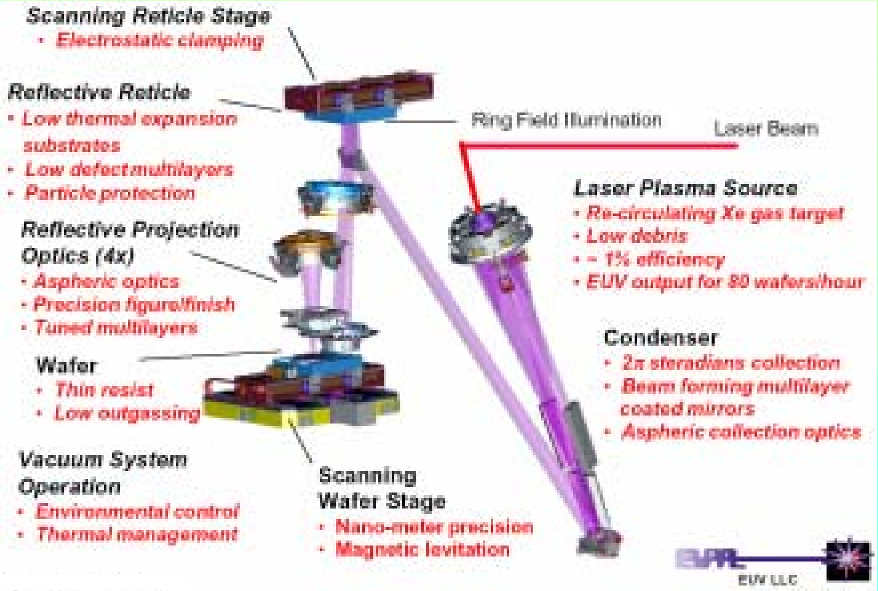
Nano-wire transistor

Future light sources:

Extreme UV

Electron beam

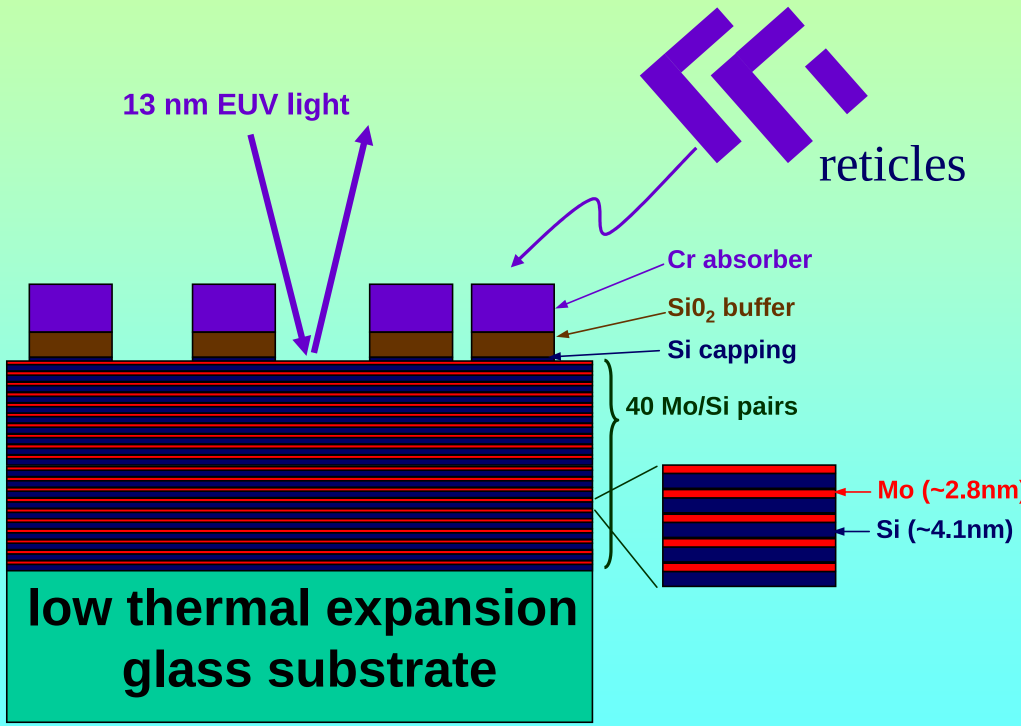
EUV exposure tool



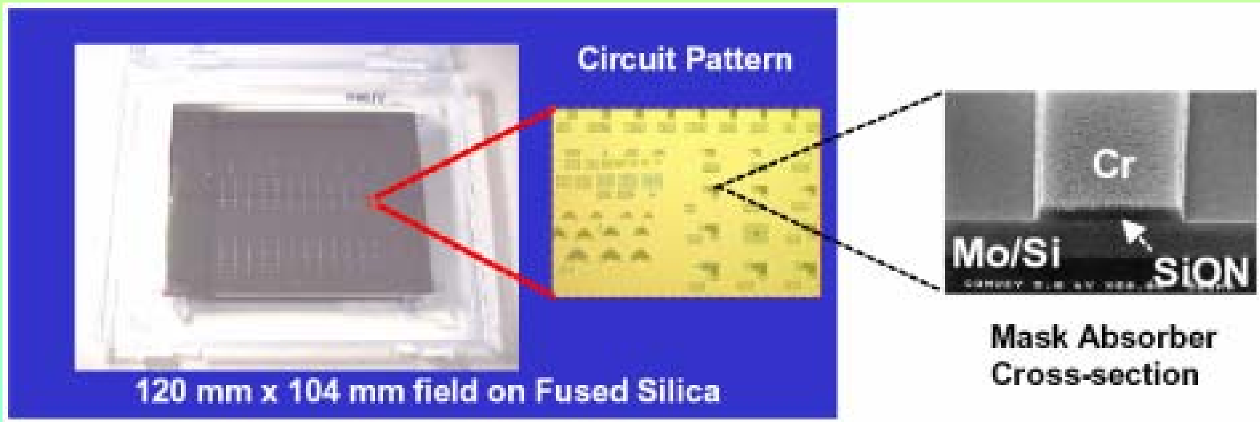
- Uses very short 13.4 nm light
- 13.4 nm radiation absorbed by all materials
- Requires reflective optics coated with quarter-wave Bragg reflectors
- Uses reflective reticles with patterned absorbers
- Vacuum operation

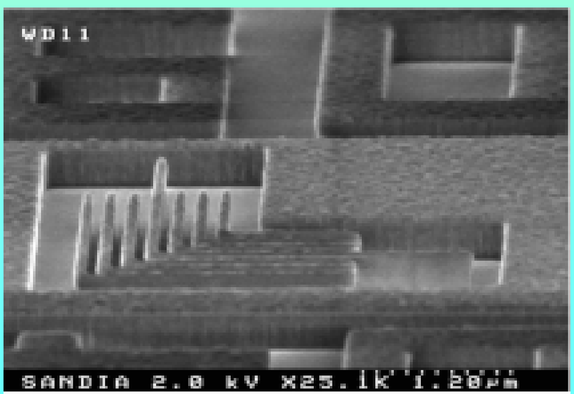
EUV reflective mask

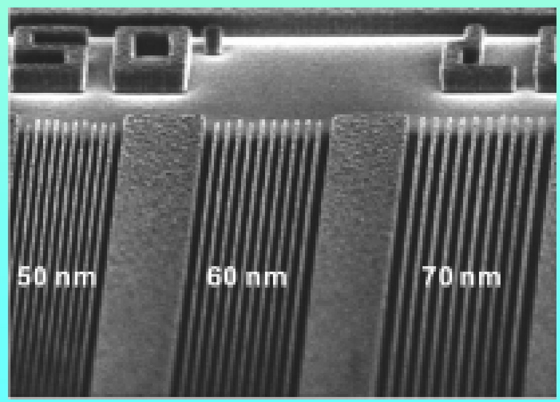
Intel EUV mask



EUV mask and patterned resist







90 nm Elbows in 350 nm polySi

Source: **Intel**

Electron-Beam Lithography

Electron Beam (e-beam) Gun:

Electrons generated by:

- Thermionic emission from a hot filament.
- Field aided emission by applying a large electric field to a filament.
- Or a combination of the two.

Filament is negatively biased (cathode) and electrons are accelerated to the substrate at typically 25 - 100 keV.

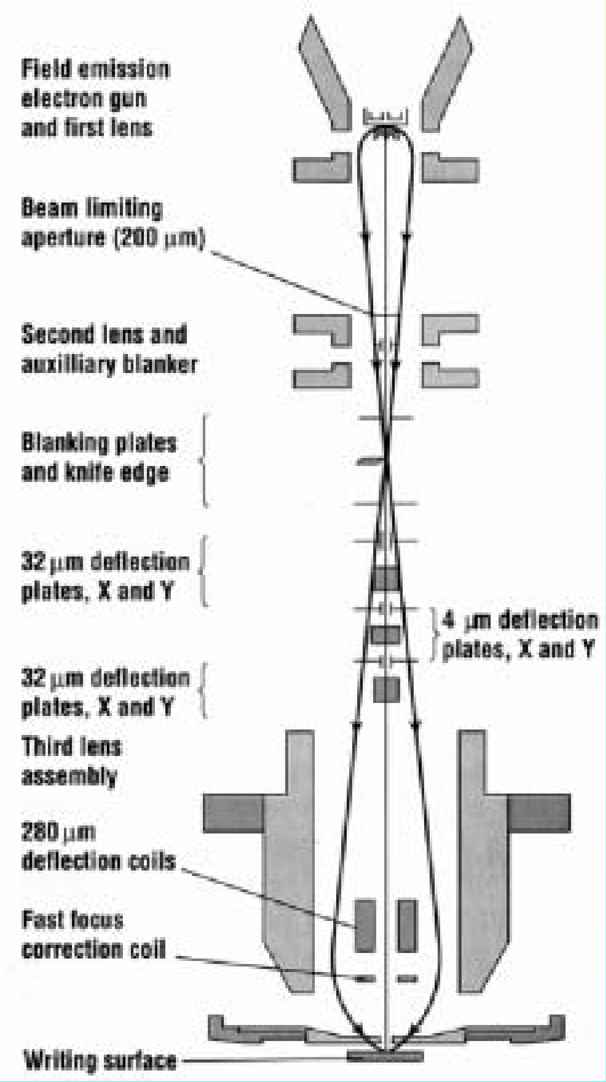
$$eV = \hbar^2 k^2 / 2m_e \Rightarrow \lambda \approx 0.25 \sim 0.12\text{nm}$$

E-beam is focused to a small spot size using:

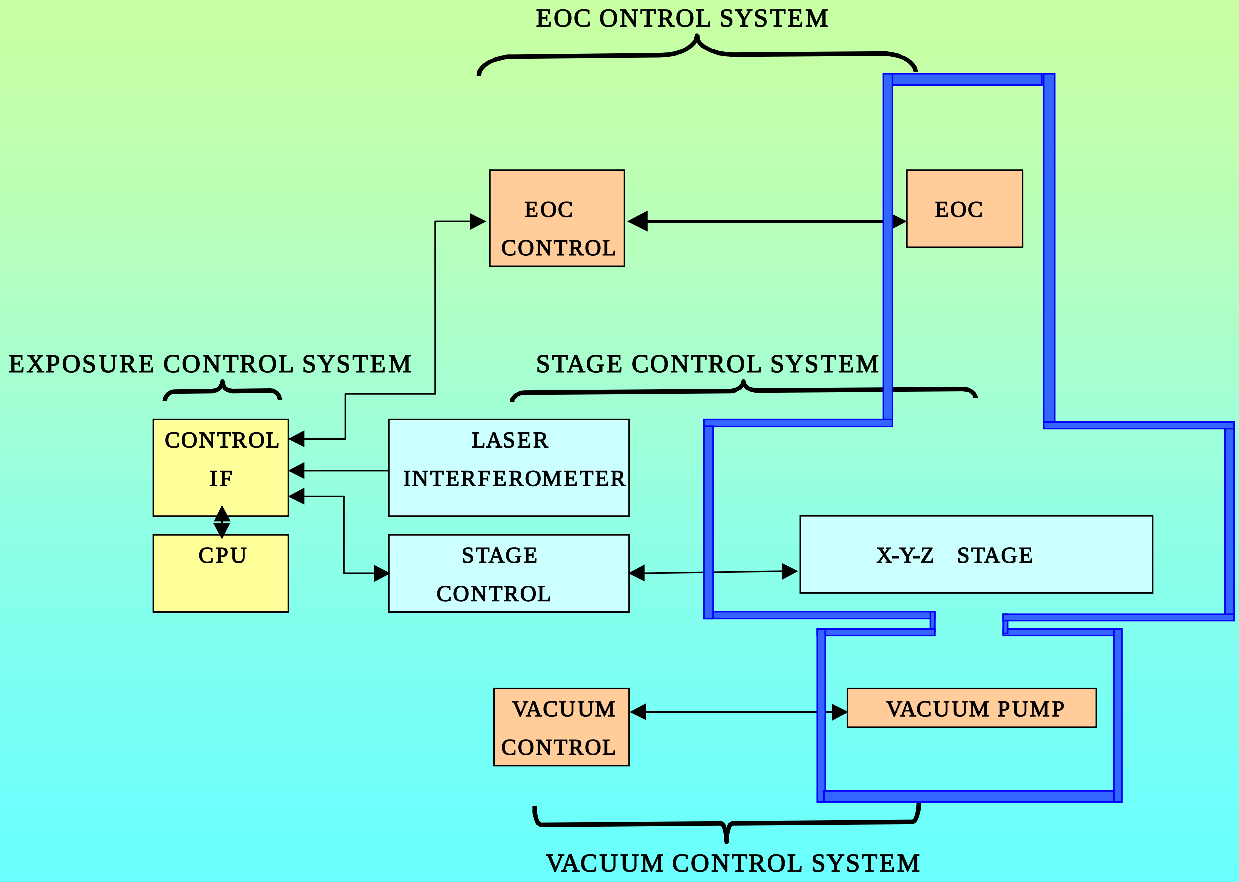
- Electrostatic lenses
- Magnetic fields
- Apertures

A scanned e-beam spot "writes" the image in the resist one "pixel" at a time.

X,Y direction of beam is controlled by electrostatic plates.



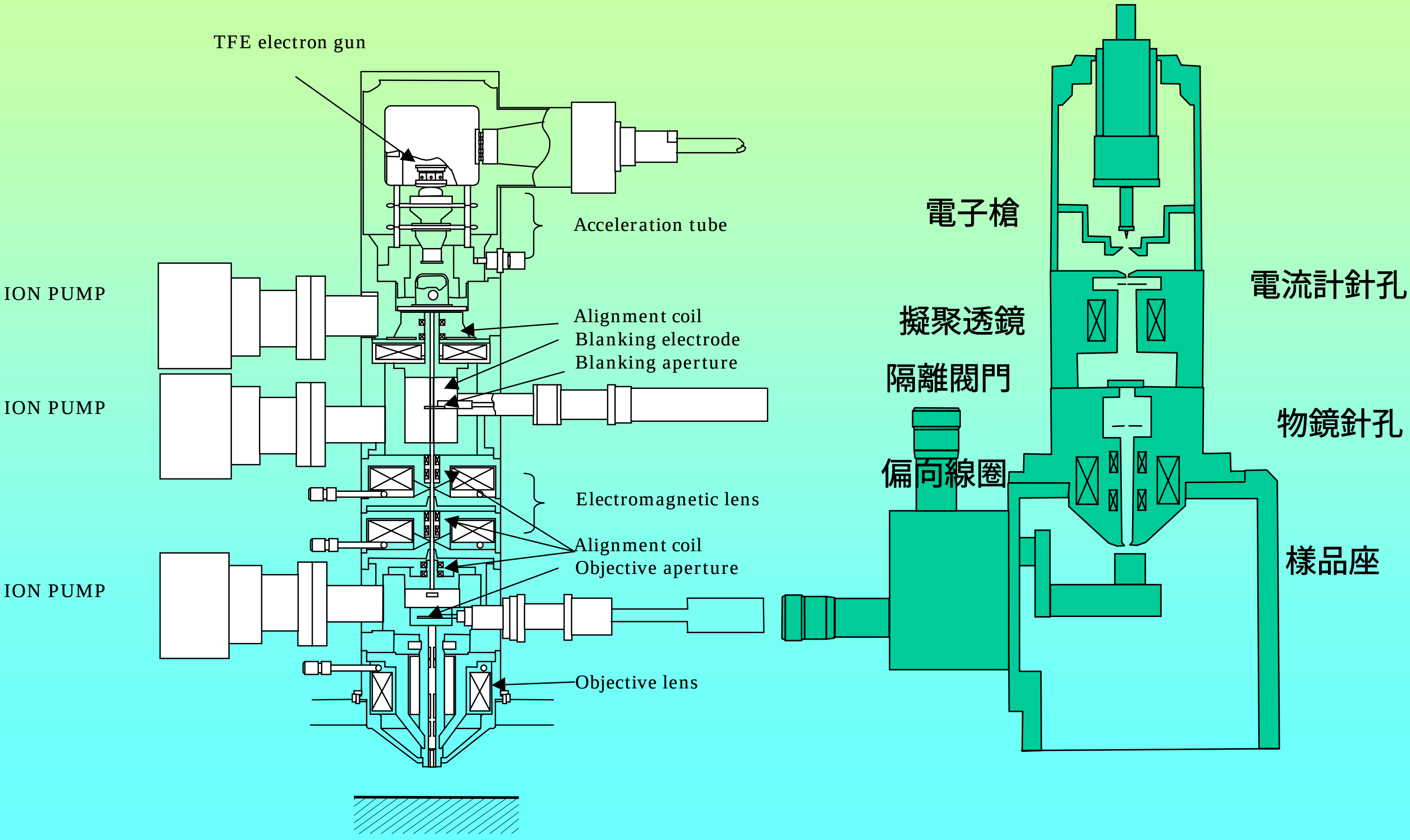
ELECTRON BEAM LITHOGRAPHY SYSTEM



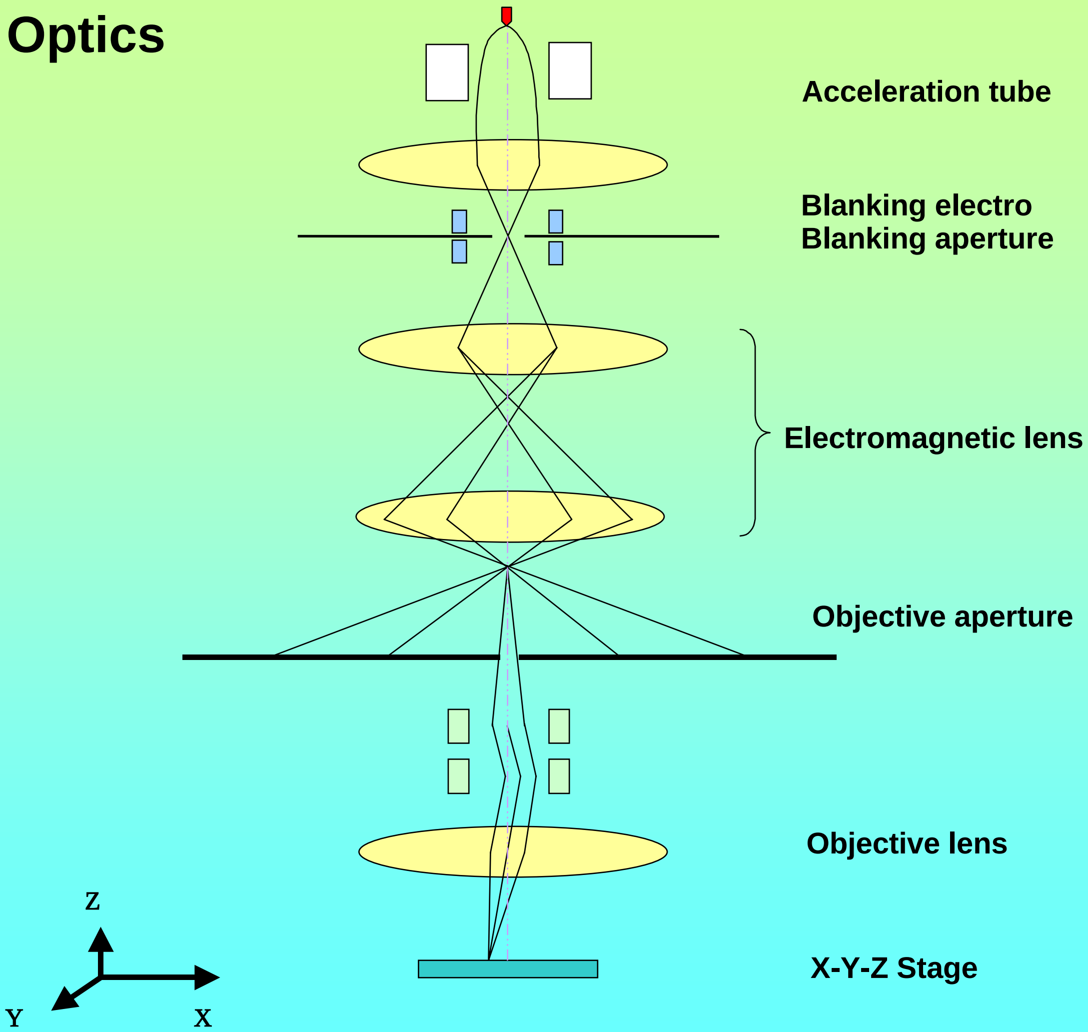
JEOL JBX-9300FS

ELIONIX ELS-7000

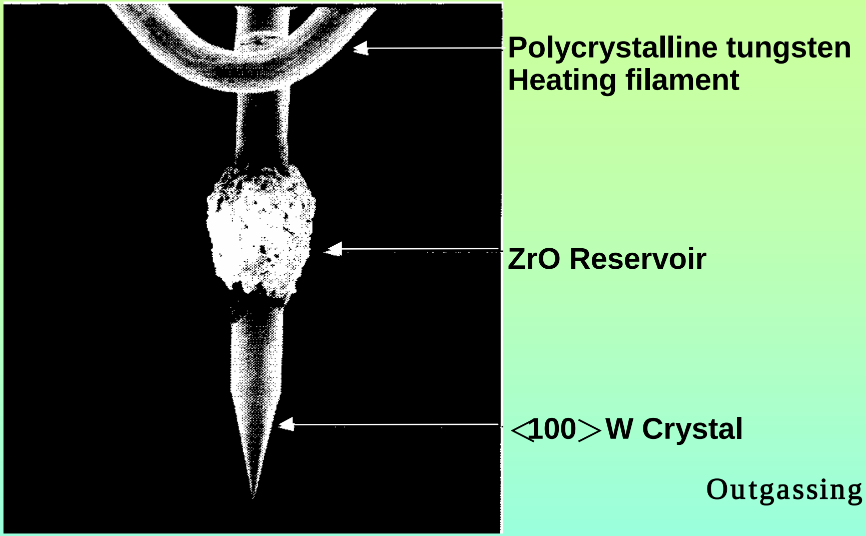
ELECTRON OPTICS SYSTEM

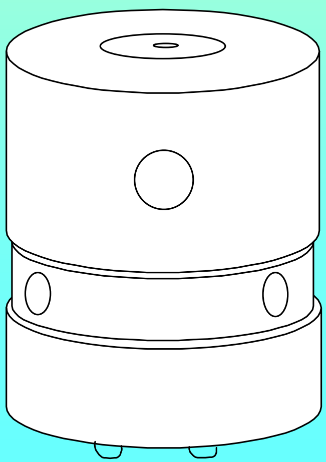


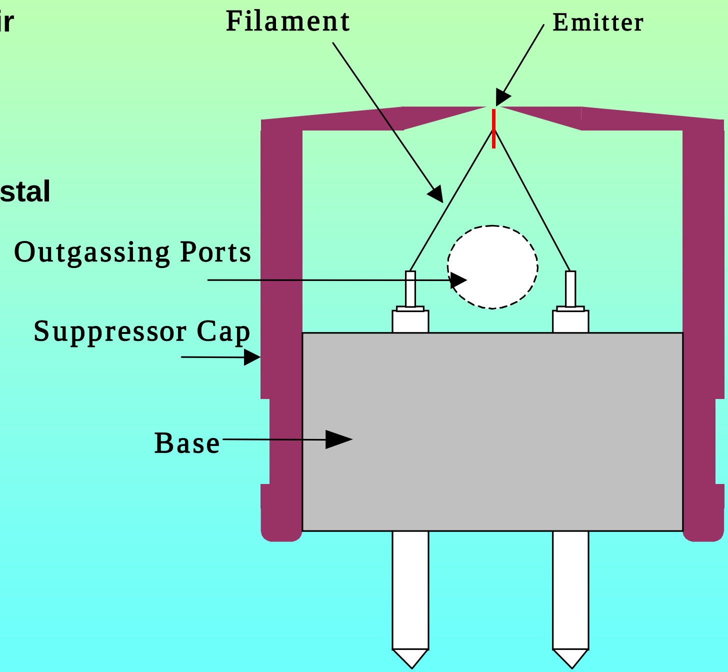
Electron Optics



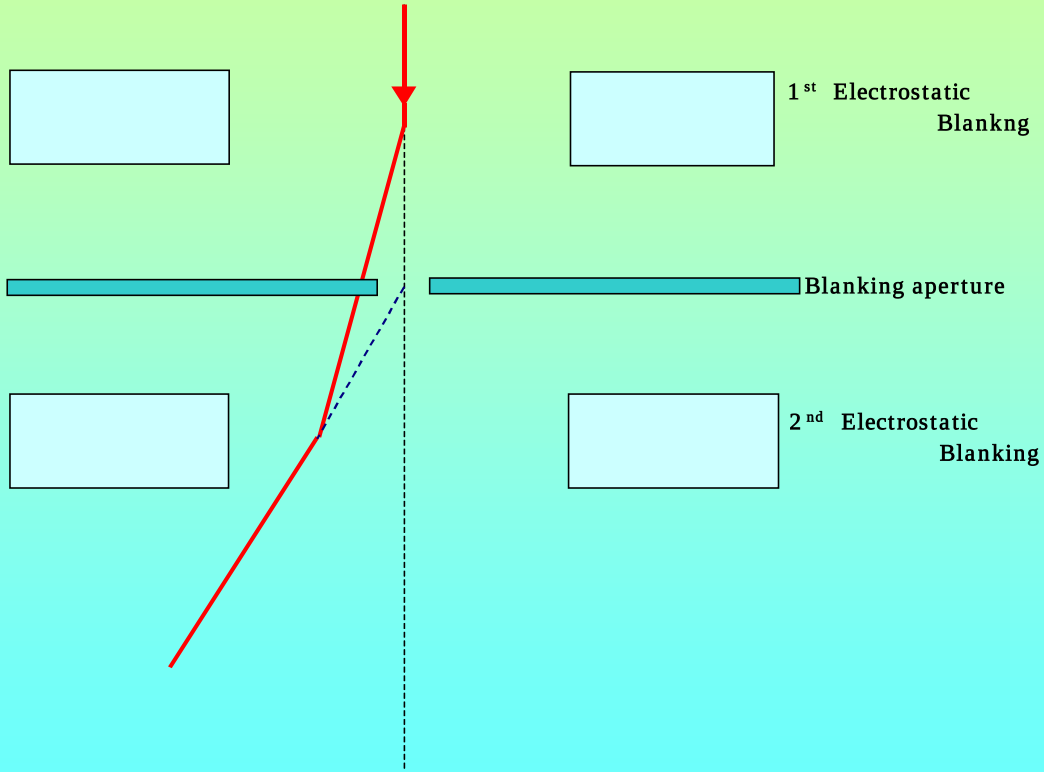
ZrO/W THERMAL FIELD EMISSION GUN



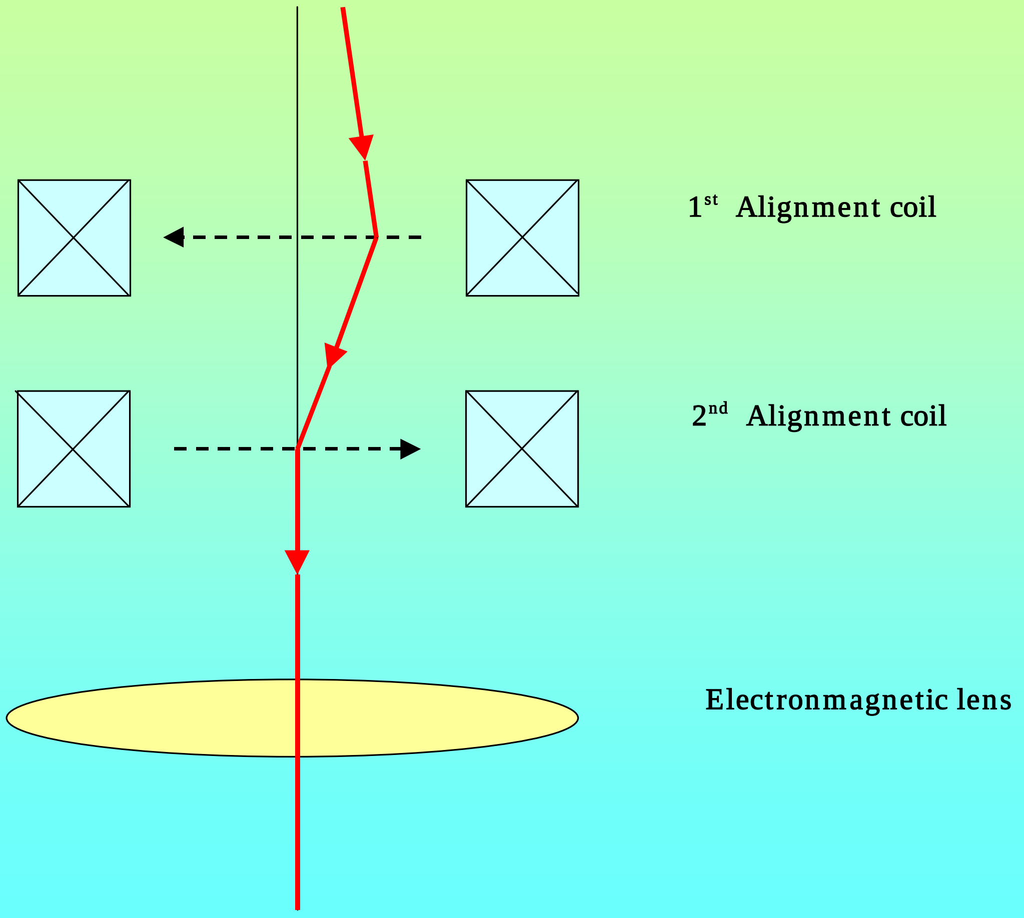




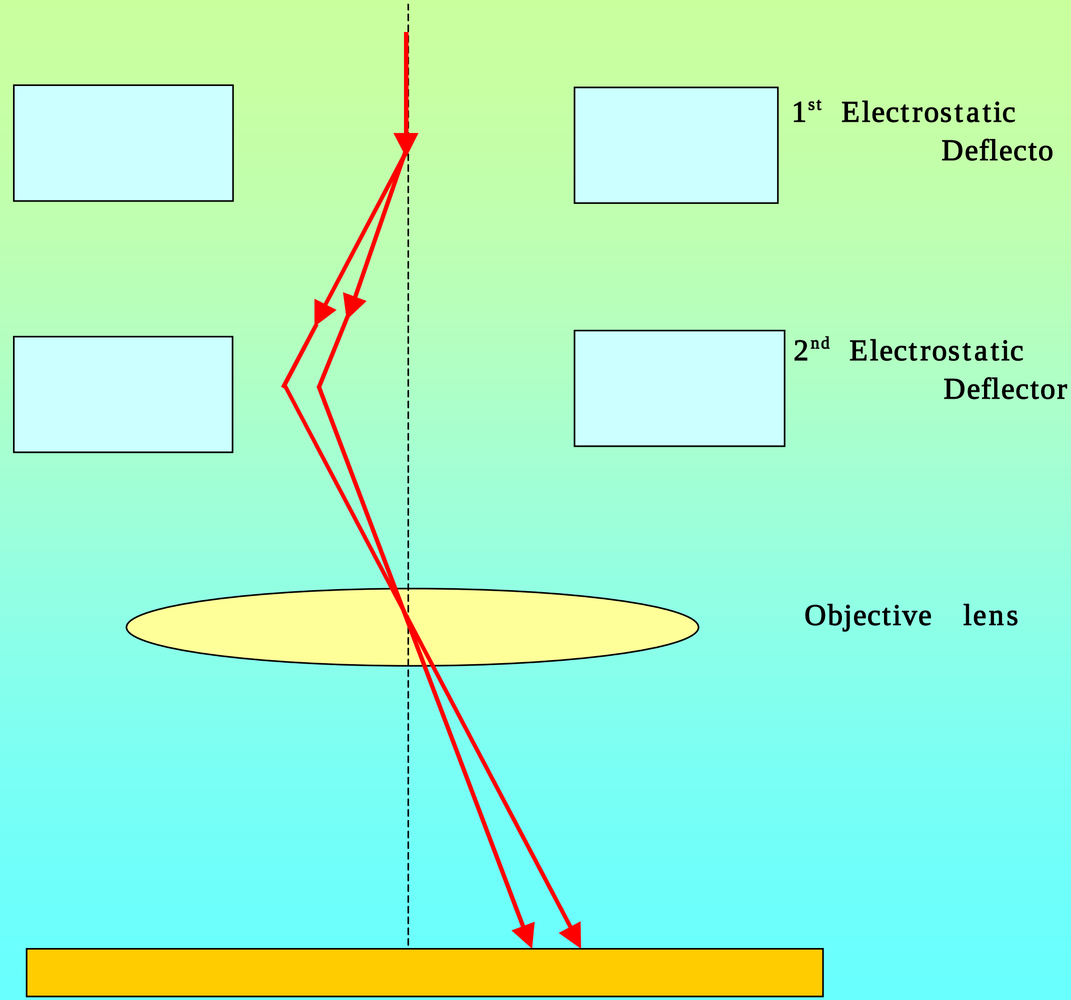
Beam blanking



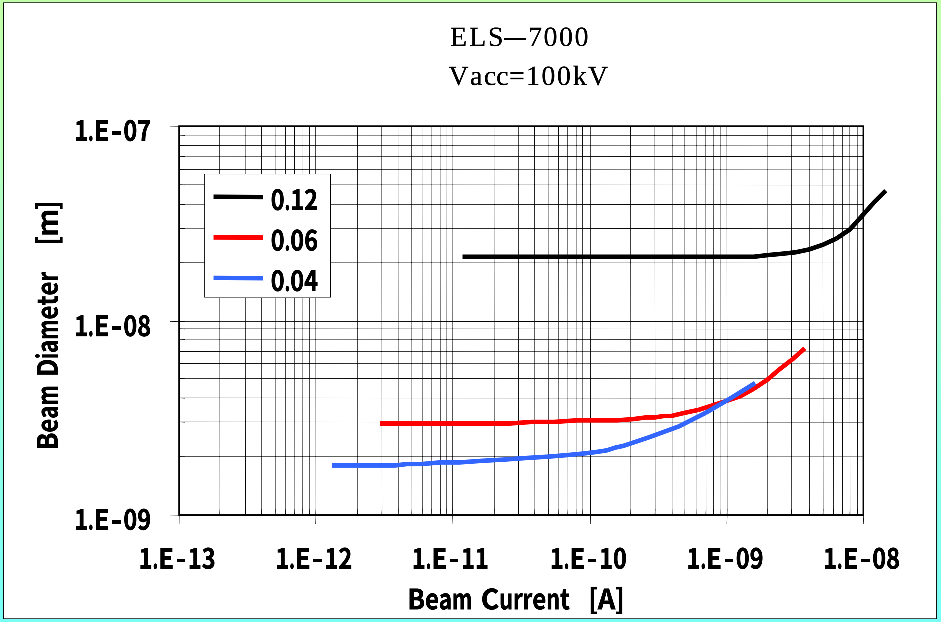
Electronmagnetic Alignment



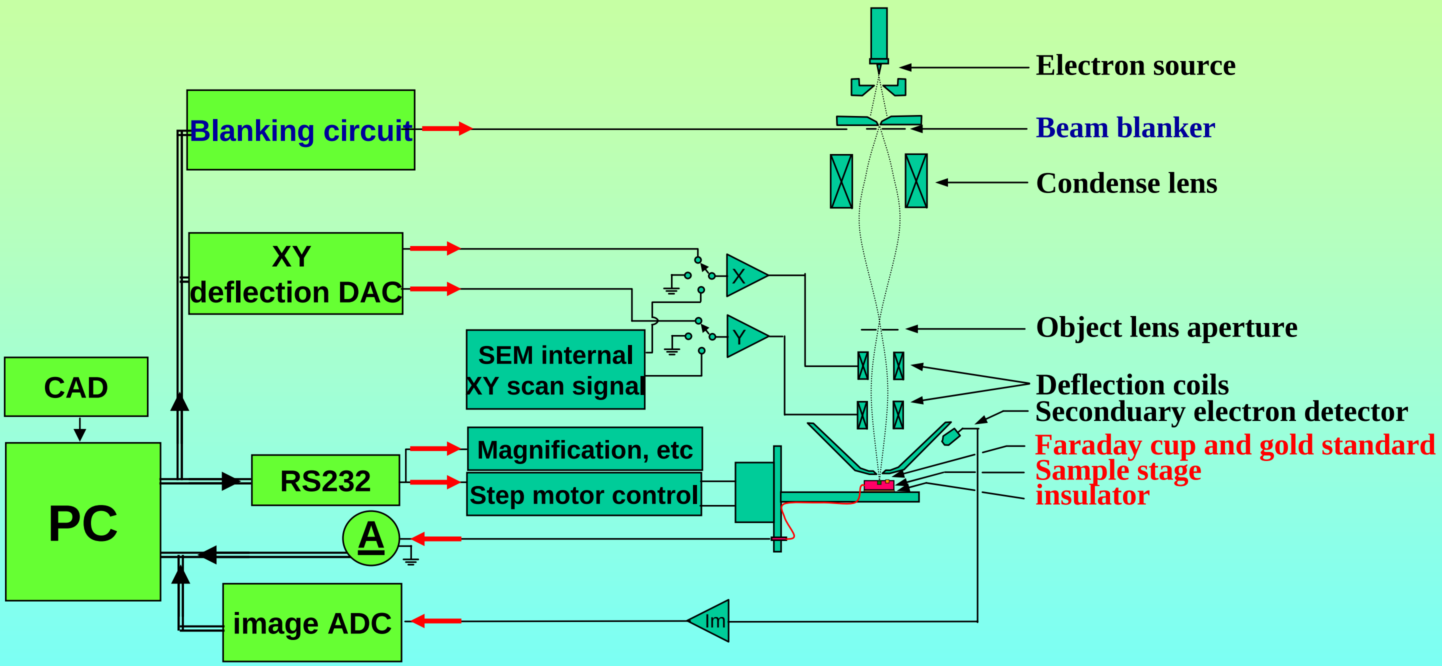
Electrostatic Deflector



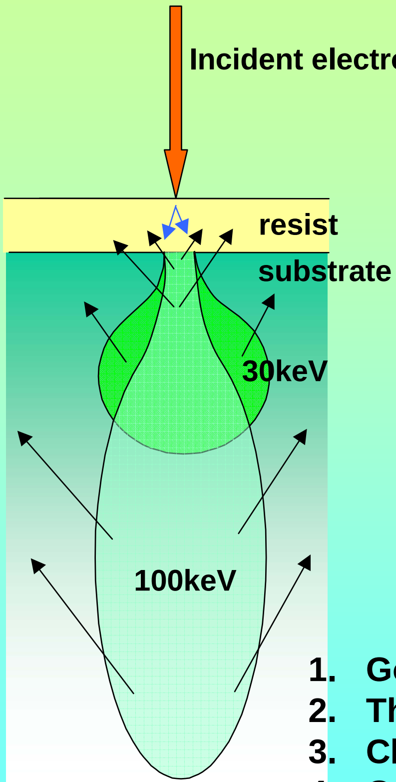
Beam spot size vs. beam current for different apertures

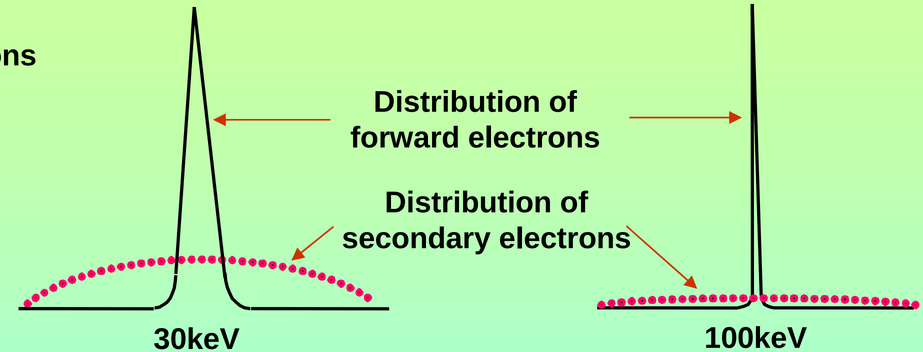


Modification of an SEM based e-beam writer



Comparison between 30keV and 100keV e-beam writer

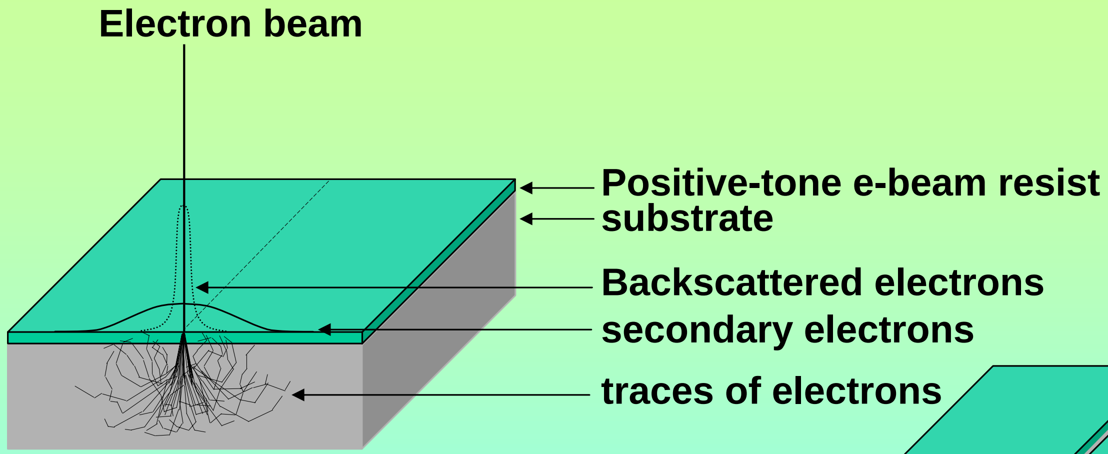


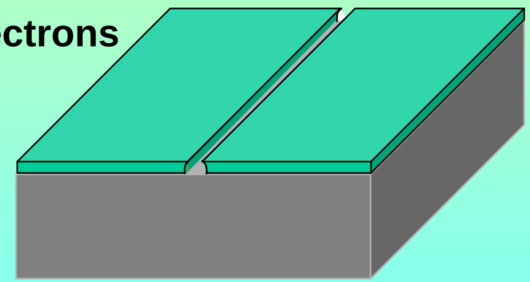


1. Good for prototype test
2. Thin resist line-width < 30nm
3. Clear align key image
4. Good for lift-off process
5. Lack of stage stability

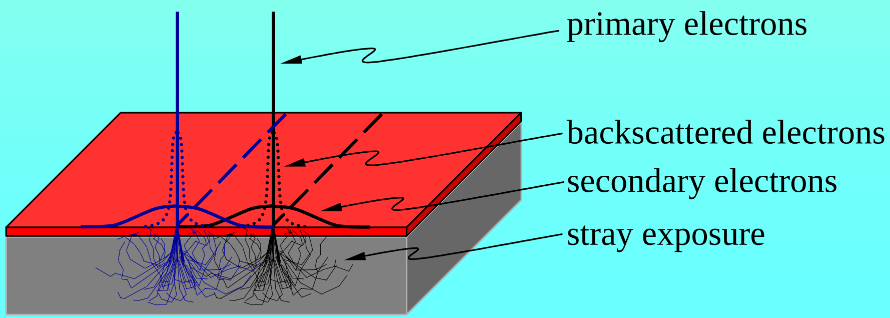
1. Good for large area exposure
2. Thin resist line-width < 10nm
3. Require thick/clear align keys
4. Require extra resist engineering
5. Stable/accurate stage stability

Principal of Electron Beam Exposure

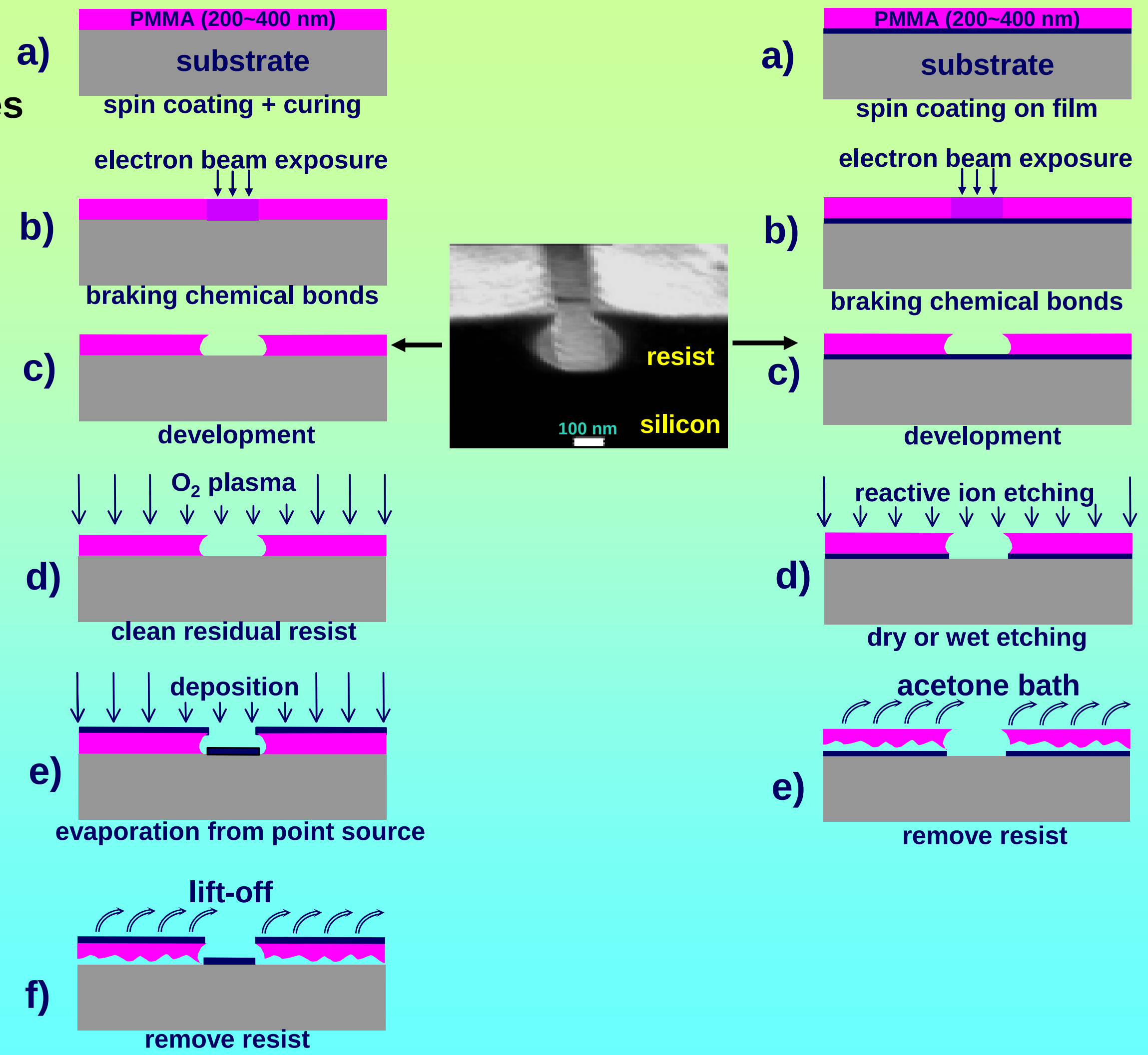




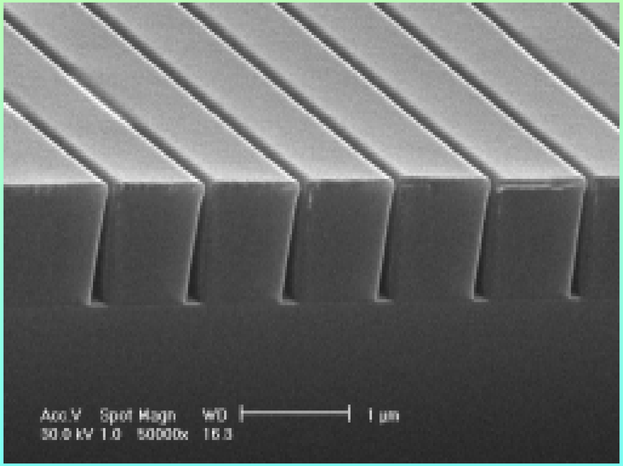
Proximity effect: main resolution limiting factor

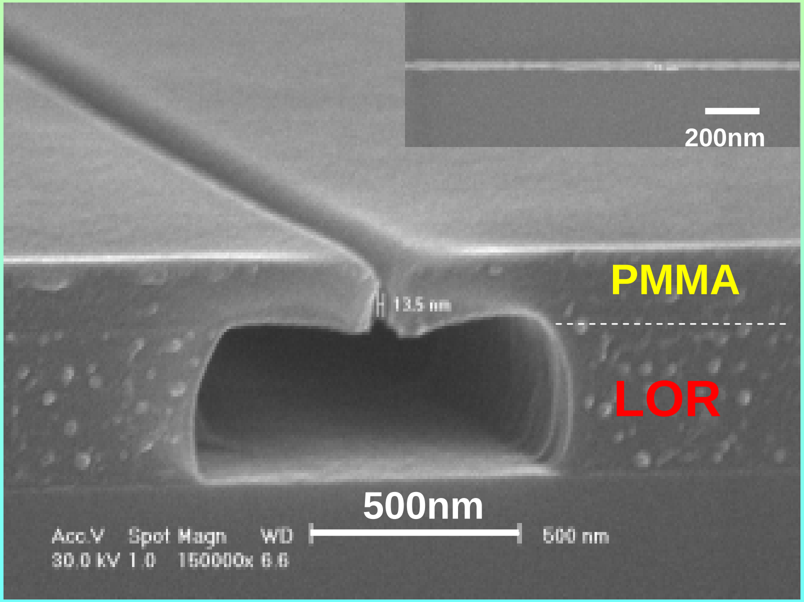


Lift-off and Etching processes

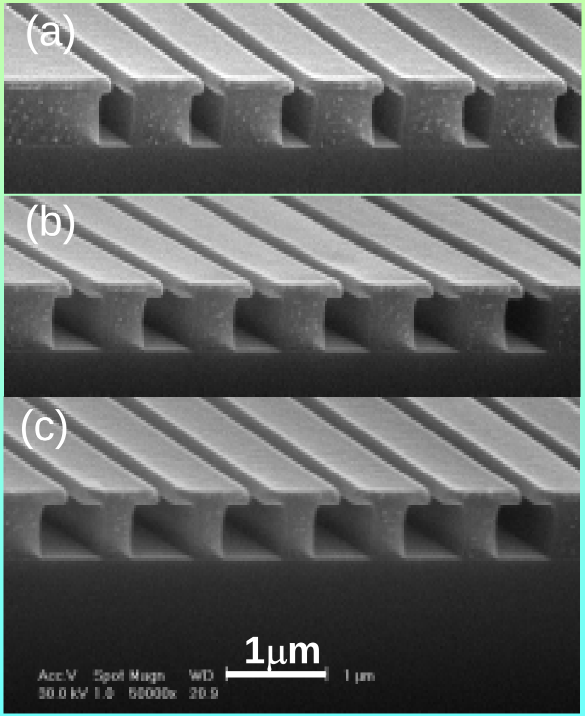


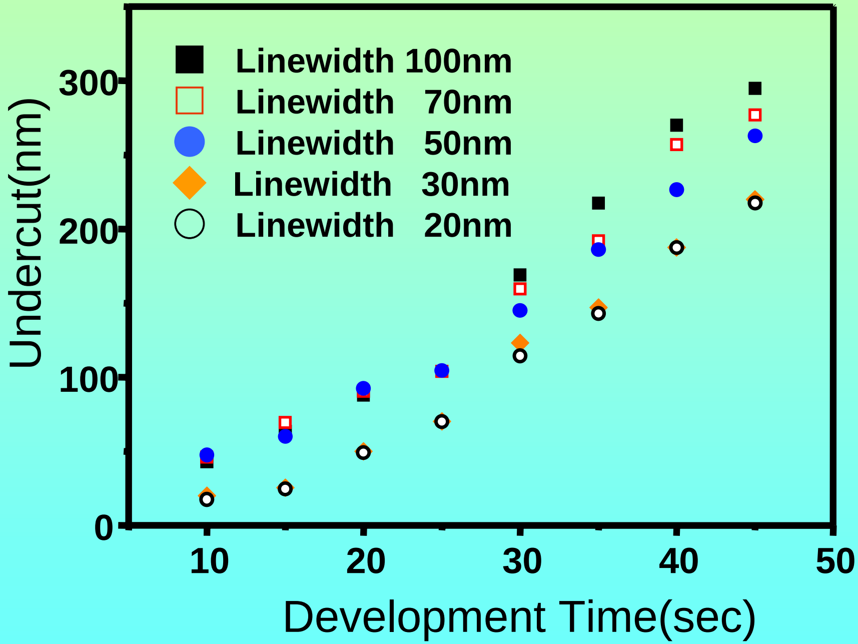
Resist profile made by high energy beam exposure



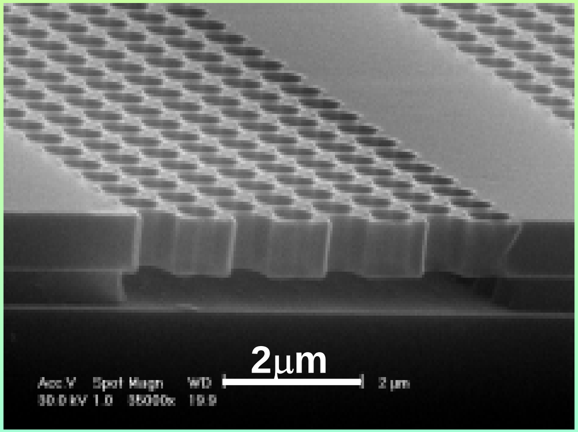


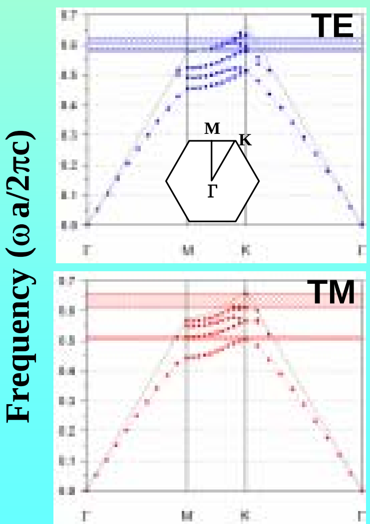
Controlling undercut in bottom layer resist



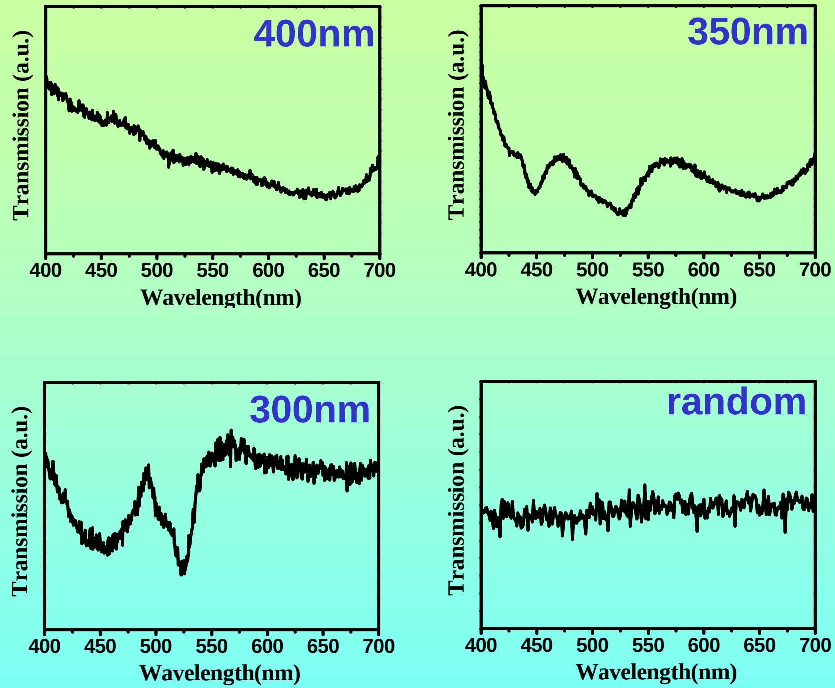


quasi-3D polymer photonic crystal

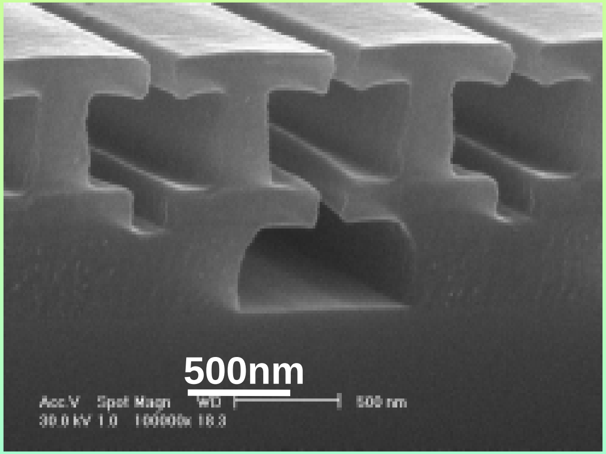


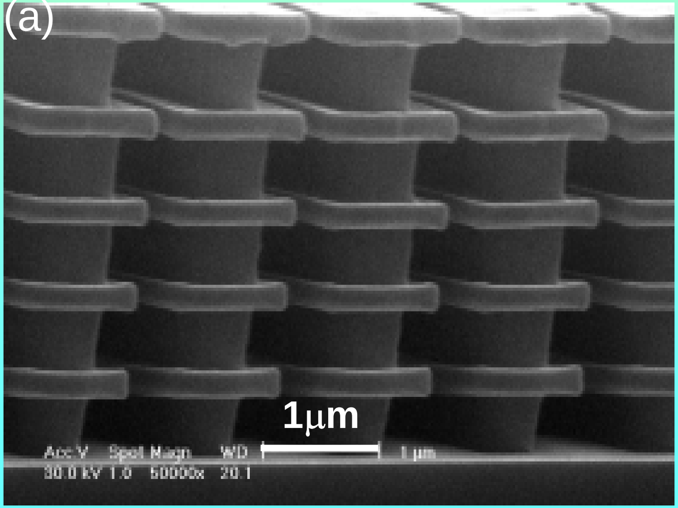


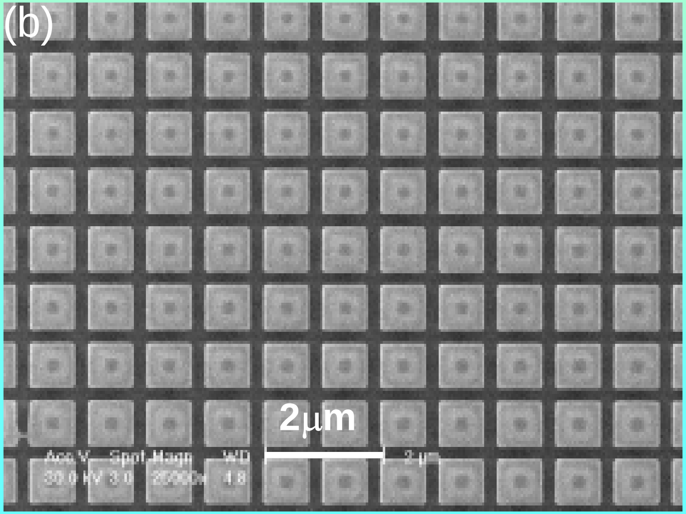
Transmission spectra, different lattice constants



3D polymer structures







Examples of 100keV e-beam lithography

3nm NiCr wire

D. R. S. Cumming et al,
Microelectronic Engineering 30 (1996), 423

Machine : Modified JEOL 100CXII

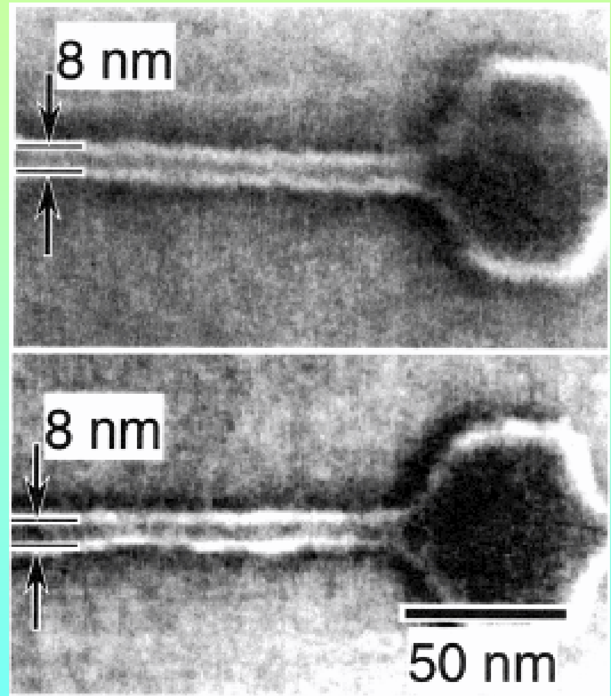
Kelvin Nanotechnology Ltd

13nm Au wire

M. Kamp et al.
J. Vac. Sci. Technol. B, 17, 86, (1999)

Machine : Eiko E 100

8 nm negative-tone inorganic resist



M. S. M. Saifullah et al., Jpn. J. Appl. Phys. **38** (1999) 7052.
K. Yamazaki et al., Proc. SPIE. **3997** (2000) 458.

Machine : 100-keV e-beam writer

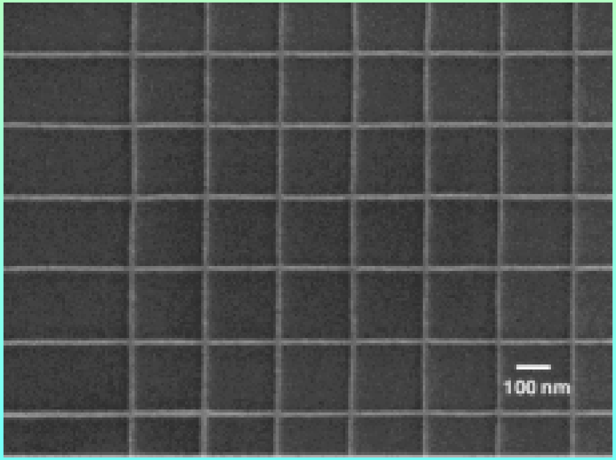
NTT Basic Research Laboratories

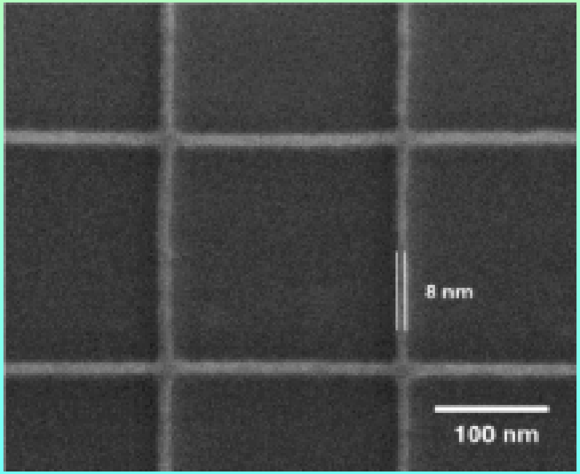
Sub-10 nm Electron Beam Nanolithography Using Spin Coatable TiO_2 Resists

University of Cambridge **and** *Leica Microsystems Lithography Limited*

Leica VB6-UHR-EWF 100keV

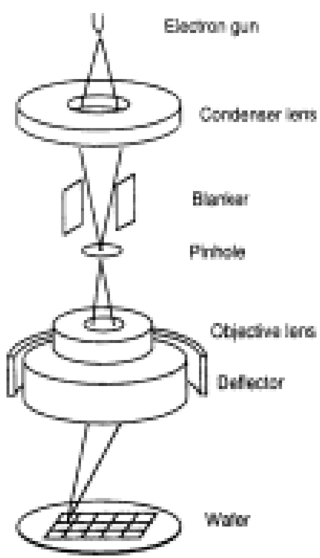
M. S. M. Saifullah,et al., Nano Letters, 3, 1587 (2003)



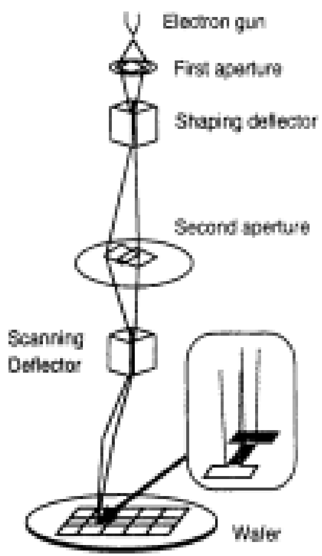


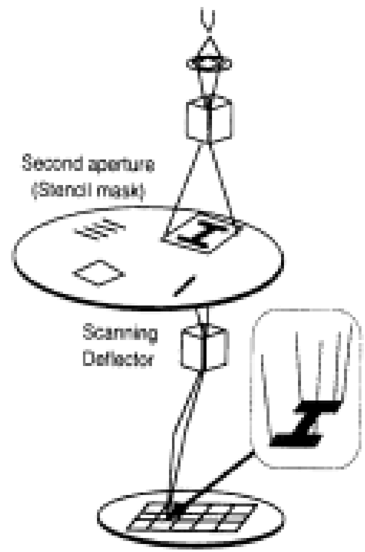
ＥＢ露光装置の用途と方式の違い

■研究開発用
　スポットビーム方式



■半導体生産用
　矩形成形ビーム方式と投影方式



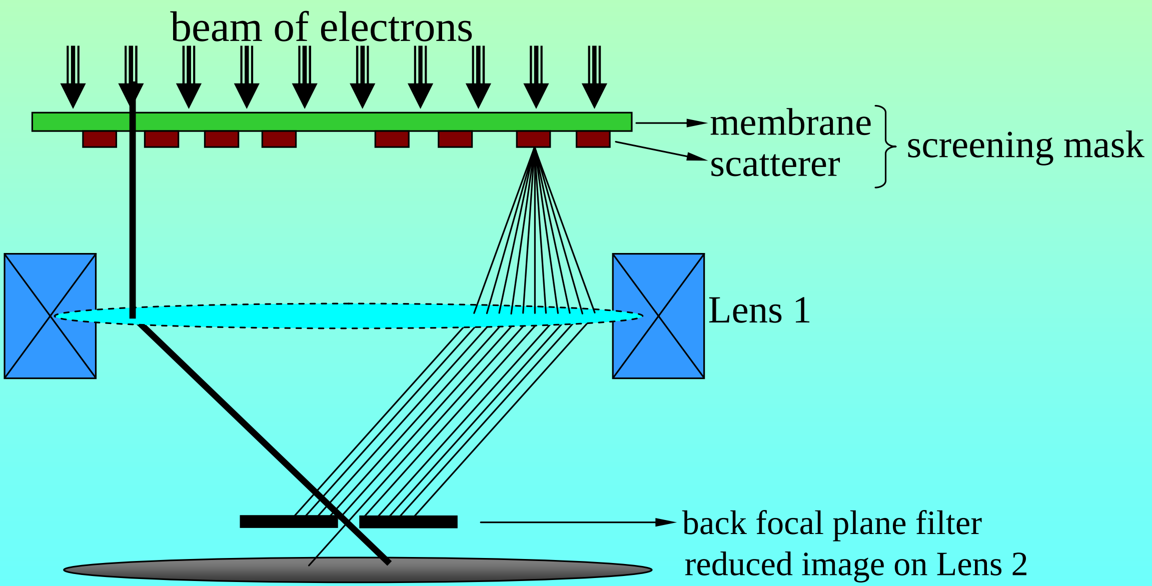


ELIONIX

- **Issues related to the integrated circuit industry:**
  - **Slow throughput**
    - A 0.1 μm diameter beam is < 10^{-12} the area of a 6” wafer.

Projection EBL Systems (SCALPEL):

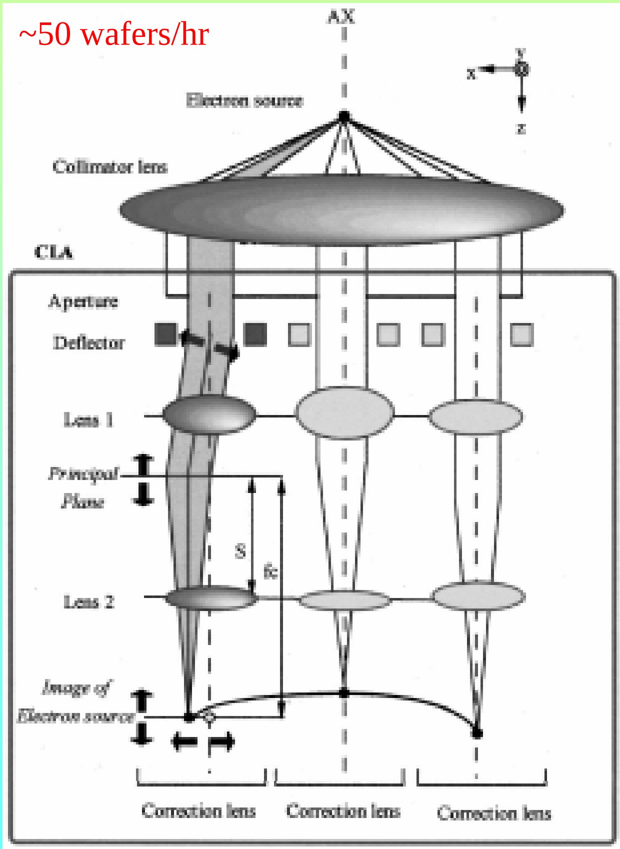
scattering with **a**ngular **l**imitation in **p**rojection **e**lectron beam **l**ithography



Multibeam direct-write electron beam lithography system

Single source with correction lens array

~50 wafers/hr

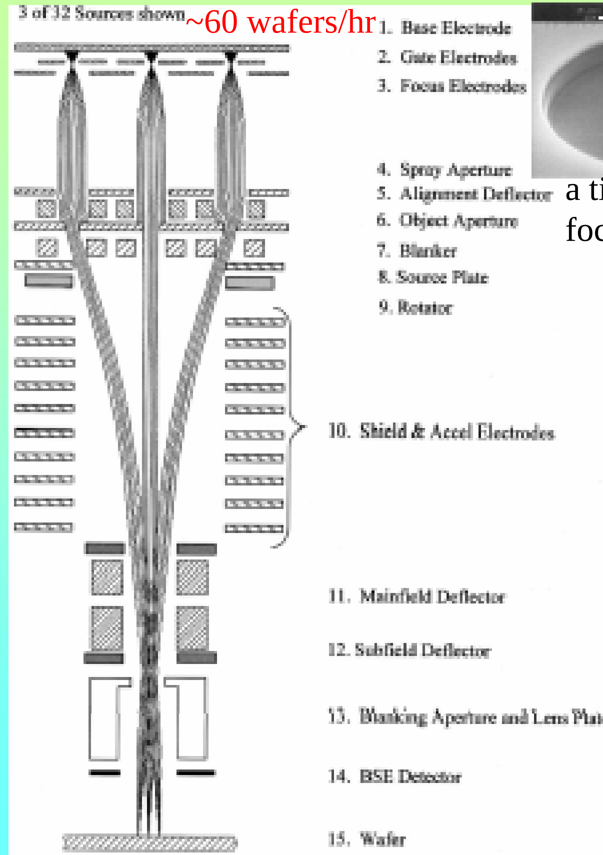


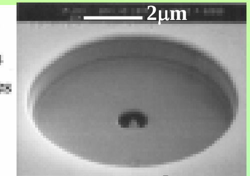
M. Muraki et al. J. Vac. Sci. Technol. B 18(6), 3061, 2000

Canon Inc.,

Multi-source with single electron optical column

~60 wafers/hr





a tip with focus electrode

E. Yin et al. J. Vac. Sci. Technol. B 18(6), 3126, 2000

Ion Diagnostics Incorporated

Take home message:

Extreme ultraviolet
electron beam projection } are considered leading contenders for next generation lithography

However, electron beam direct write system is a maskless lithography.

- eliminating mask amortization costs and
- speed up chip development cycles.

The ultimate resolution of electron beam lithography remains to be explored

Main applications:

- manufacture of small volume specialty products
- direct write for advanced prototyping of integrated circuits
- studies of quantum effects and other novel physics phenomena at very small dimensions